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New PFC design using Multiple Buck Converters

Doaa S. Mohammed
Computer Engineering Department,
Al-Rasheed University College
Baghdad, Iraq

***Abstract*—This paper presents a new design of a power factor correction (PFC) technique with a step down dc-dc buck converter. This research proposes PFC that adopts voltage-controlled parallel-connected buck converters. The parallel connection structure increases the power level, enhances the overall efficiency and power system reliability. However, unequally current distribution between converters is a major problem which may lead to inductor saturation and even destroy the converters which handles the larger current. For this reason, a suitable control scheme used to overcome this issue.**

A suitable control scheme is suggested for the parallel connected buck converters. An average control scheme is suggested for the PFC system. In this scheme, the output current of each converter tracks the average load current which is the ratio of the load current to the number of parallel-connected converters. This scheme is a modular but needs only one information which is the number of parallel-connected converters to be shared between converters. A mathematical analysis is performed to examine the system performances including current distribution between the parallel-connected converters and stability of proposed PFC. The analysis reflects the system stability and shows the possibility of maintaining even current distribution between the converters. A Simulation results show the excellent performance of the PFC with an equally current distribution between converters.

Keywords—PFC; buck; dc-dc converter; ac-dc; pwm.

I. INTRODUCTION

Electrical power converters is a very important part of industry. Ac-dc converters (rectifiers) are used as a major part for switched mode power supplies, uninterrupted power supplies (UPS), battery chargers [1]. For these reasons, ac-dc converters have attracted a great deal of attention and several commercial ac-dc converters have been developed. A main problem with ac-dc converters is a power factor (PF). Besides power losses, PF causes harmonics that travel down the neutral line and disrupt other devices connected to the AC mains line. This reason has prompted researchers to develop several custom versions and a lot of researches have been carried out to design and implement PFC.

One scheme of PFC that suggested to use dc-dc converter (like buck, boost, Fly back,..,etc.) as a PFC, is placed after the rectifier stage and before the output storage capacitor [2,3,4]. In general, PFC can be either a passive PFC or active PFC. A simple way to enhance power factor of the rectifiers is by adding a passive filter after it. These passive filters could be built from capacitors and inductors. Although the passive filters is simple in design and control, but it suffering from the high inductors current and high capacitors voltage. Also a passive filter has a bulky sizes of capacitors and inductors [5, 6]. An active PFC built on a switching electronic devices like, MOSFETs, IGBTs.

A conventional step-down buck converter is shown in Fig. 1, it regulates an input voltage to give an output voltage smaller than input.

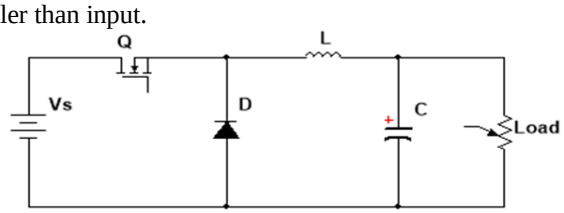

Fig. 1. Dc-dc buck converter.

This research present a modular PFC built on paralleled voltage control buck converters. This feature will enhance the reliability and overall system efficiency. Furthermore, the ripple of the output current and voltage will be decrease [7].

II. PROPOSED PFC

A. Main circuit

A proposed PFC with multiple dc-dc converters is shown in Fig. 2. Where two voltage controlled step down buck dc-dc converters are supplied from same source (output of the rectifier) and connected in same output. A main problem with the parallel connection of dc-dc converters is unequally current distribution between converters which may lead to inductor saturation and even destroy the converters which handles the larger current. To avoid this problem a duty cycle of the two converters (D_m) is modified. In basic words, a total output current from the paralleled converters is sensed and divided by 2 (2 is the number of the converters that connected in parallel). This new current are compare with each individual converter current to give a new duty cycle (D_{new}) that add to the main duty cycle to give a modified duty cycle (D) that equal in two converters to share equal current in each converter.

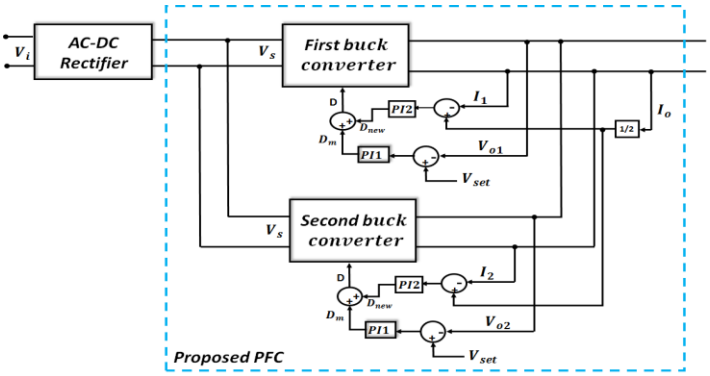

Fig. 2. A proposed PFC with multiple dc-dc converters.

B. Mathematical analysis

The schematic diagram of the conventional buck converter is shown in Fig. 1 and the j^{th} modeling for the closed loop

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voltage control is shown in Fig. 3. A switching voltage drop could be represent as V_{sw} in the modelling [8]. And it's a main effect of the unequally sharing current between converters.

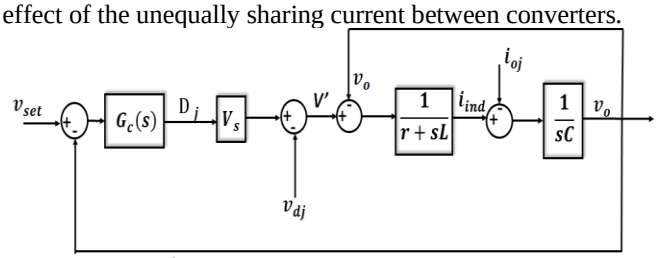

Fig. 3. j[th] modeling for the closed loop voltage control.

From fig. 3 above the closed loop transfer functions could be written as below:

$$G_1 = \left.\frac{v_o(s)}{v_{set}(s)}\right|_{v_{dj},i_{oj}=0} = \frac{G_c V_s}{s^2LC + srC + 1 + G_c V_s};$$

$$G_2 = \left.\frac{v_o(s)}{i_o(s)}\right|_{v_{set},v_{dj}=0} = \frac{sL + r}{s^2LC + srC + 1 + G_c V_s};$$

And

$$G_3 = \left.\frac{v_o(s)}{v_{dj}(s)}\right|_{v_{set},i_{oj}=0} = \frac{1}{s^2LC + srC + 1 + G_c V_s}$$

So, the output voltage equation could be arrange to be:

$$v_o(s) = v_{setj}(s)G_1(s) - i_{oj}(s)G_2(s) - v_{dj}(s)G_3(s) \quad (1)$$

Where Gc is a transfer function of PI controller, and it equal to:

$$G_c = k_p + (k_i/s)$$

From (1) the output current could be written as below:

$$i_{oj} = 1/G_2\left[v_{setj}G_1 - v_{dj}G_3 - v_o\right] \quad (2)$$

So, the converters individual currents will be:

$$i_{o1} = 1/G_2\left[v_{set1}G_1 - v_{d1}G_3 - v_o\right]$$
$$i_{o2} = 1/G_2\left[v_{set2}G_1 - v_{d2}G_3 - v_o\right]$$

That lead to average current that between converters will be:

$$i_{avg} = \frac{1}{G_2}\left[v_{set\_avg}G_1 - v_o - v_{d\_avg}G_3\right] \quad (3)$$

To find current that circulated between converters, sub. (3) from (2) :

$$i_{avg} - i_{oj} = \frac{1}{G_2}\left[\left(v_{set\_avg} - v_{setj}\right)G_1 - \left(v_{d_{avg}} - v_{dj}\right)G_3\right] \quad (4)$$

The converters are connected in parallel, so:

$$v_{set1} = v_{set2} = v_{setj} = v_{set\_avg} \quad (5)$$

Then (4) could be written as:

$$i_{avg} - i_{oj} = G_3/G_2\left[\left(v_{dj} - v_{d_{avg}}\right)\right] \quad (6)$$

When the two converters are connected in parallel, the model of the buck converters will be as shown in Fig. 4.

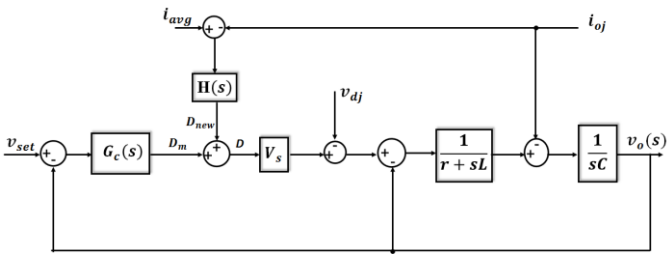

Fig. 4. Buck converter model for the Proposed PFC.

A new closed loop transfer function will be:

$$G_{new} = \frac{H(s)V_s}{s^2LC + srC + 1 + G_c V_s} \quad (6)$$

Then, the output voltage will be:

$$v_o(s) = G_{new}\left(i_{avg} - i_{oj}\right) + v_{set}(s)G_1(s) - v_{dj}(s)G_3(s) - i_{oj}(s)G_2(s)$$

The output current will be as below:

$$i_{oj} = 1/(G_2 + G_{new})\left[v_{set}G_1 - v_{dj}G_3 + i_{avg}G_{new} - v_o\right] \quad (7)$$

To find current that circulated between converters,

$$i_{av} - i_{oj} = 1/(G_2 + G_5)\left[\left(v_{dj} - v_{d_{av}}\right)G_3\right] \quad (8)$$

III. SIMULATION RESULTS

A. *Parallel operation*

To validate that an equal current share in the both buck converter according to our design, a Simulink model for only two paralleled buck converters is built in a MATLAB Simulink program. Fig. 5 shows the waveforms of the output currents for the two paralleled buck converters with the total load current, when the load equal to 15Ω. It clear that the suggested sharing control method is excellent in control by make the two converters have a same value. Fig. 6 shows the waveforms of the output currents for the two paralleled buck converters with the total load current, when the load equal to 150Ω. It also shows that the suggested sharing control method is excellent in control by make the two converters have a same value. Then, when the load resistance equal to 300Ω, the suggested control method work excellent and the currents waveforms that shown in the Fig. 7. From the results above, our current sharing control method was work very good and give an excellent sharing among the two buck converters.

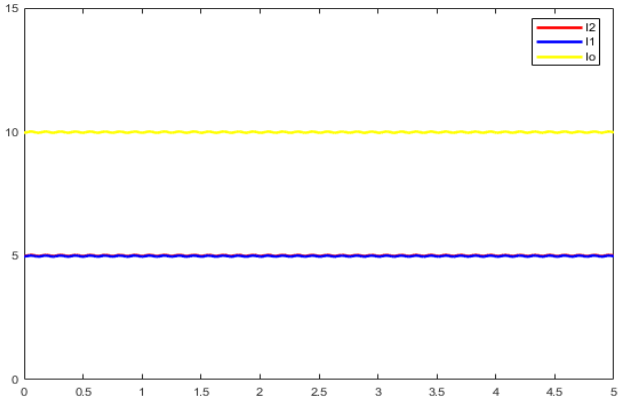

Fig. 5. Waveforms of the output converters currents at 15Ω.

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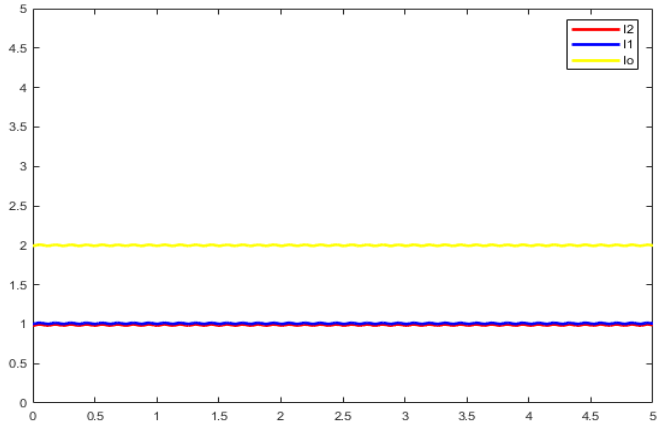

Fig. 6. Waveforms of the output converters currents at 150Ω.

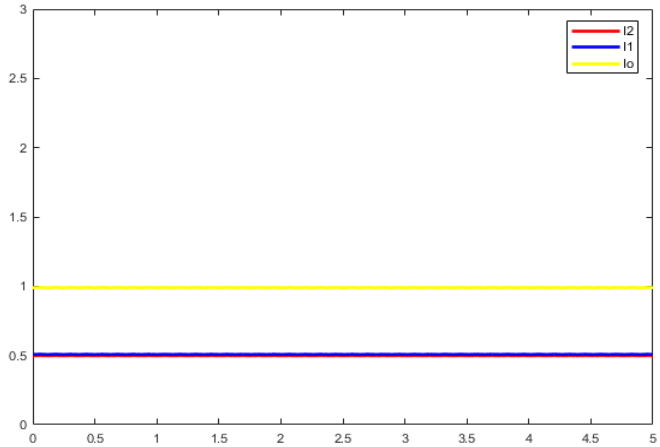

Fig. 7. Waveforms of the output converters currents at 300Ω.

B. Proposed PFC simulation results

After successful parallel operation simulation tests of the power stage of the PFC. In order to validate designed PFC, a simulation made by using MATLAB Simulink program. Fig. 8 shows a steady state waveforms of the input voltage and current at full load operation (750w). The waveforms are sinusoidal and the total harmonic distortion (THD) is about 3% and the input power factor 0.999. Fig. 9 shows the input waveforms at load equal to 200w, and it's clear that the THD is about 10% and the input power factor equal to 0.990. With different loads a PF is calculated and write down before and after using our suggested PFC and the comparison result is shown in the Fig. 10.

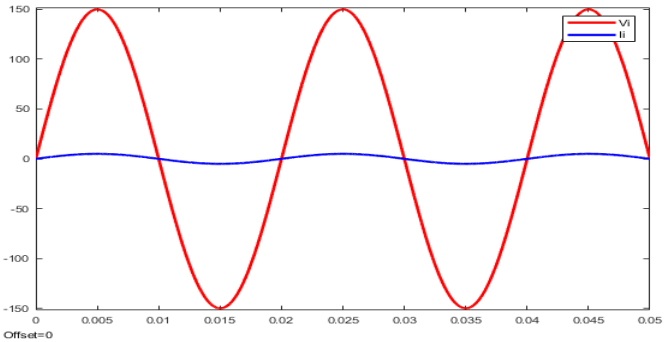

Fig. 8. Inputs voltage and current waveforms at load equal 750w.

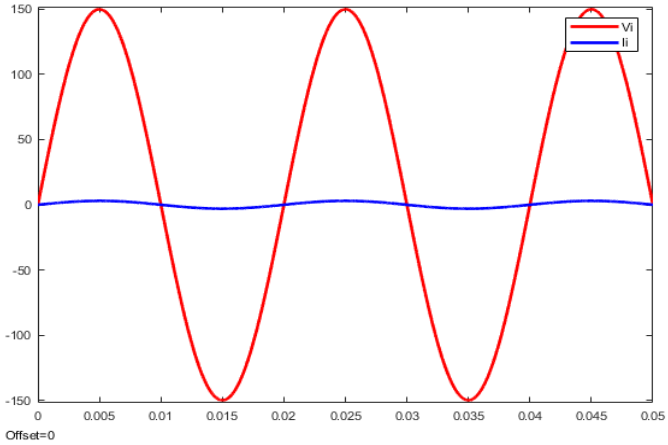

Fig. 9. Inputs voltage and current waveforms at load equal 200w.

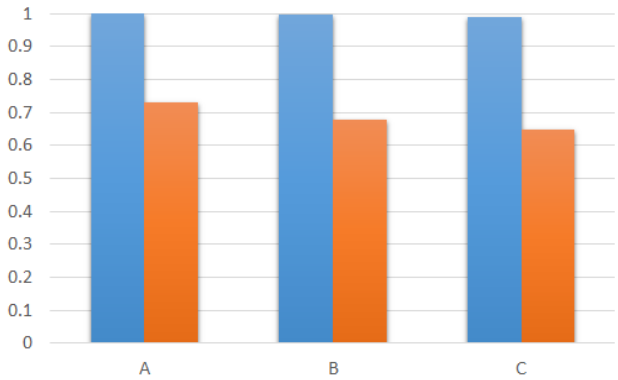

Fig. 10. A calculated PF before and after using our suggested PFC.

IV. CONCLUSION

A new design of PFC is discussed through this paper by using a multiple step down buck converters that connected in parallel. At the first, a main problem of unequally current sharing between the converters is analysis and solved mathematically and by simulation. A simulation results gave us an excellent behavior to go ahead to apply our design to the rectifier. Then, an overall power system with suggested PFC and rectifier are built in a Mat lab Simulink. A simulation results show a good power factor correction compared with the power factor of the system without PFC connected as that shown in the Fig. 10. A good idea for future work is to prove that the design of parallel operation is modular by connect more than two buck converters in parallel.

REFERENCES

[1] H.Z.Azazi, E. E. EL-Kholy, S.A.Mahmoud and S.S.Shokralla, "Review of Passive and Active Circuits for Power Factor Correction in Single Phase, Low Power AC-DC Converters‖," International Middle East Power Systems Conference (MEPCON'10),Cairo University, Egypt, December 19-21, 2010.

[2] D. S. Chen and J.-S. Lai, "A Study of Power Correction Boost Converteroperating at CCM-DCM Mode," in Proc. IEEE Southeastcon, vol. 93, pp. 6-13, 1993.

[3] V. Grigore and J. Kyyra, "High Power Factor Rectifier Based on Buck Converter Operating in Discontinuous Capacitor Voltage Mode," in Proc. IEEE Appl. Power Electron. Conf. Expo., Mar. 1999, pp. 612-618.

[4] W. Tang, Y. Jiang, G. C. Hua, F. C. Lee and I. Cohen, "Power Factor Correction with Fly back Converter Em-ploying Charge Control in APEC'93 Rec., pp. 293-298.

International Journal of Engineering Research & Technology (IJERT)
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[5] N. Mohan, T. M. Undeland, W. P. Robbins, "Power Electronics: Converters, Applications, and Design," New York, NY, USA, John Wiley & Sons, Inc., 1995.
[6] Supratim Basu, "Single Phase Active Power Factor Correction Converters Methods for Optimizing EMI, Performance and Costs," PhD. Thesis, Chalmers University of Technology, Göteborg, Sweden, June 2006.
[7] L. de la Torre, "High Frequency High Efficiency DC/DC-Converters," in Proceedings of the 1995 European Conference on Power Electronics and Application, Seville, pp.2.106-2.110.
[8] Y. Zhang, S. Duan, Y. Kang, and J. Chen, "The Restrain of Harmonic Circulating Currents between Parallel Inverters," 5th International Power Electronics and Motion Control Conference, pp. 1-5, 2006.