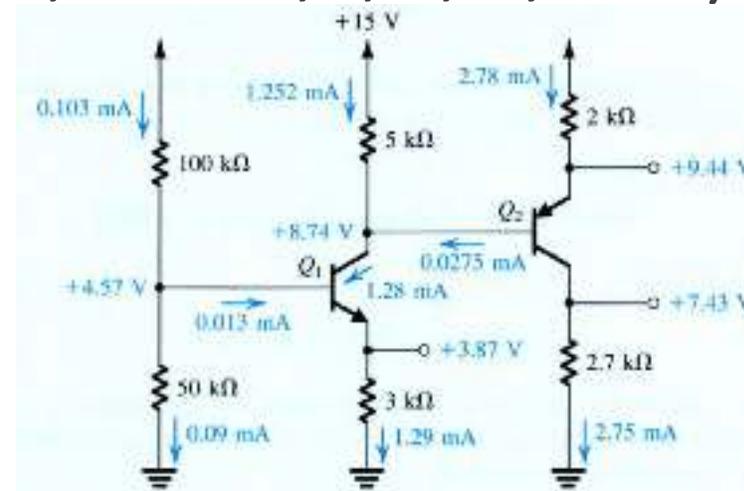
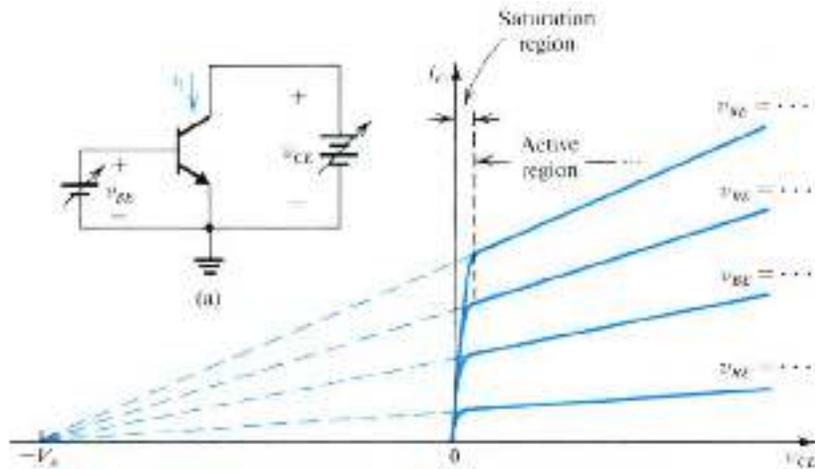


# Electronics-I Course Layout

- Electronics (active devices; diodes and transistors)
  1. Analysis (for a given circuit, find V, I, P, Z, etc.)



2. Design (from a specification design: amplifier, logic gate, driver, voltage regulator, etc.)

# Semiconductor Materials

- Semiconductors are a special class of elements having a **conductivity** between that of a good **conductor** and that of an **insulator**.

$$\text{Resistance } R = \rho \frac{l}{A} [\Omega]$$

- Conductivity  $\sigma = 1/\rho$

Sigma

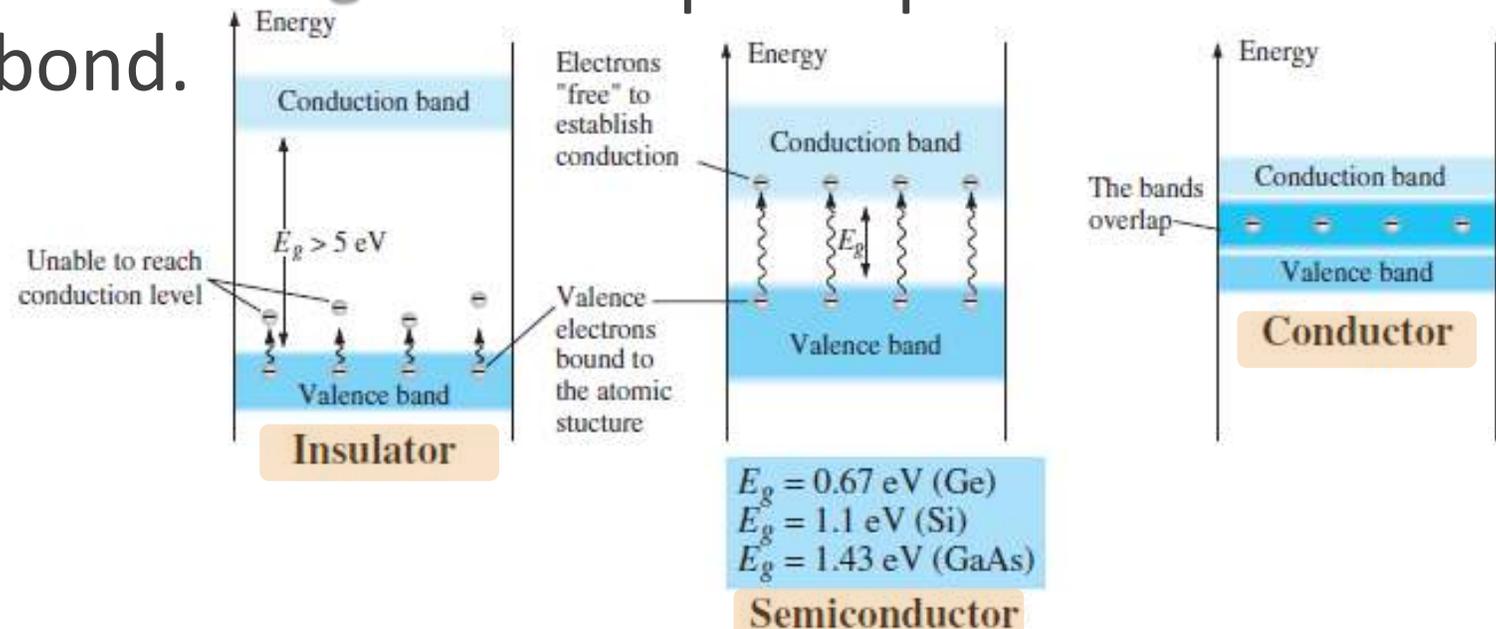
Rho

Material	Resistivity $\rho$ [ $\Omega \cdot m$ ] @ 20 °C
Silver (Ag)	$1.59 \times 10^{-8}$
Copper (Cu)	$1.68 \times 10^{-8}$
Gallium Arsenide (GaAs)	$5 \times 10^{-7}$ to $10 \times 10^{-3}$
Germanium (Ge)	$4.6 \times 10^{-1}$
Silicon (Si)	$6.40 \times 10^2$
Wood (oven dried)	$1 \times 10^{14} \rightarrow 1 \times 10^{16}$
Teflon	$10 \times 10^{22} \rightarrow 10 \times 10^{24}$

# Semiconductor Materials (cont'd)

- Ge, Si, and GaAs are the three **semiconductors** used most frequently in the construction of electronic devices.
- **Valence** electron is an  $e$  that can participate in the formation of a chemical bond.

1eV=1.6×10<sup>-19</sup> Joule

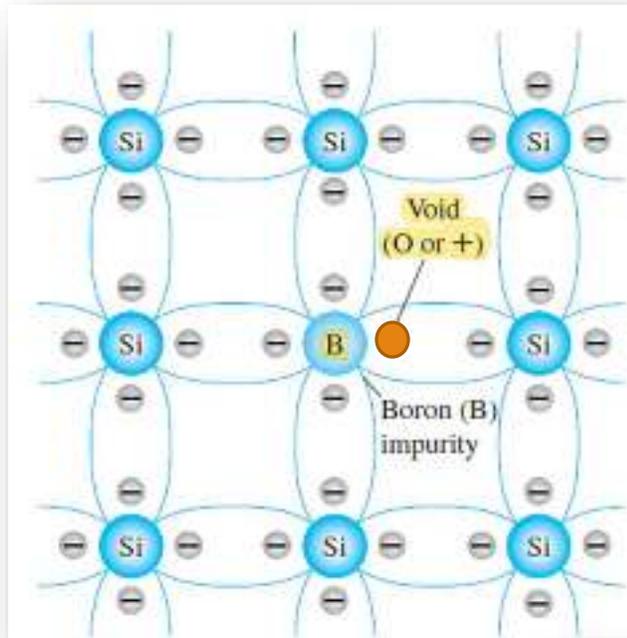


# Semiconductor Materials (cont'd)

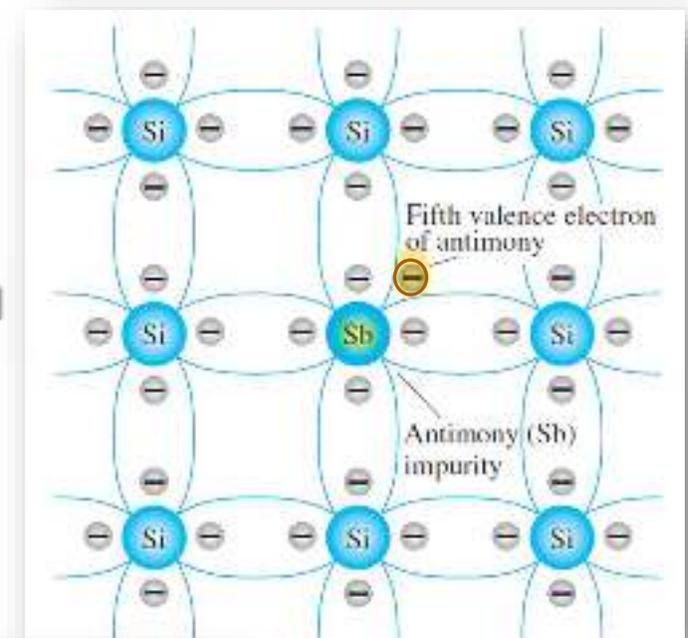
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- **Si** is used **most frequently** as the **base material** in the construction of **solid-state** electronic devices.
- The characteristics of a semiconductor material can be **altered significantly** by adding specific **impurity** atoms to the **relatively pure** semiconductor material.
- **Boron (B)**, having **3 valence** electrons, and **Antimony (Sb)**, having **5 valence** electrons are the doping impurities used with **Si**.

# Semiconductor Materials (cont'd)

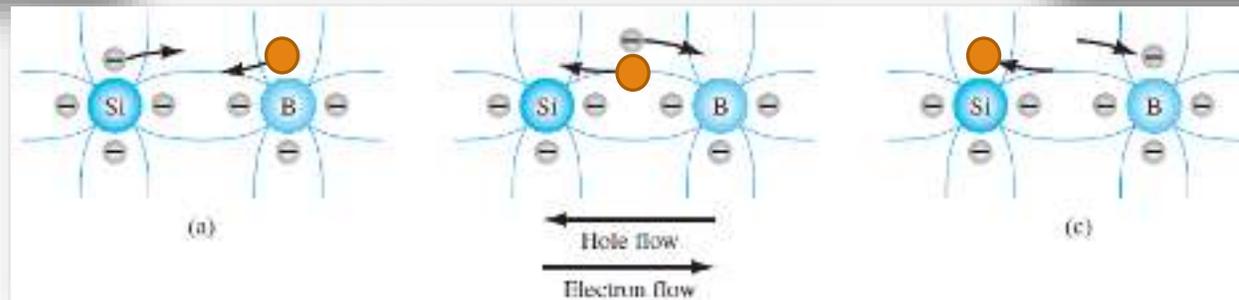


p -Type Material



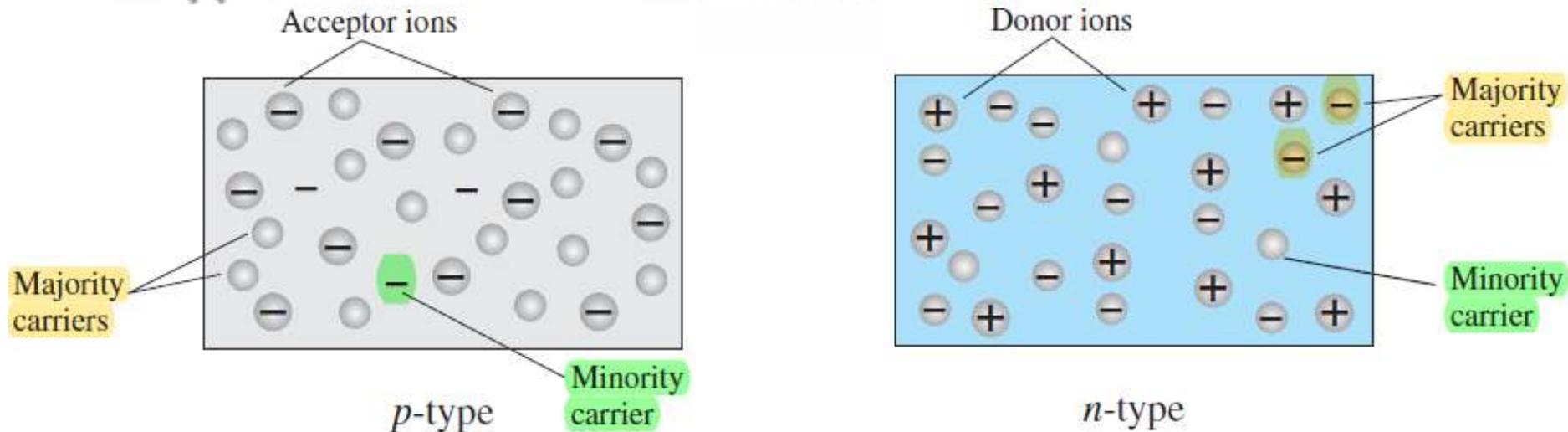
n -Type Material

Electron vs. conventional flow



# Semiconductor Materials (cont'd)

- The **n-type** and **p-type** materials represent the basic building blocks of semiconductor devices.
- In an **p-type** material, the **hole** is the **majority** carrier, while in **n-type** material, the **electron** is the **majority** carrier.



# Outline

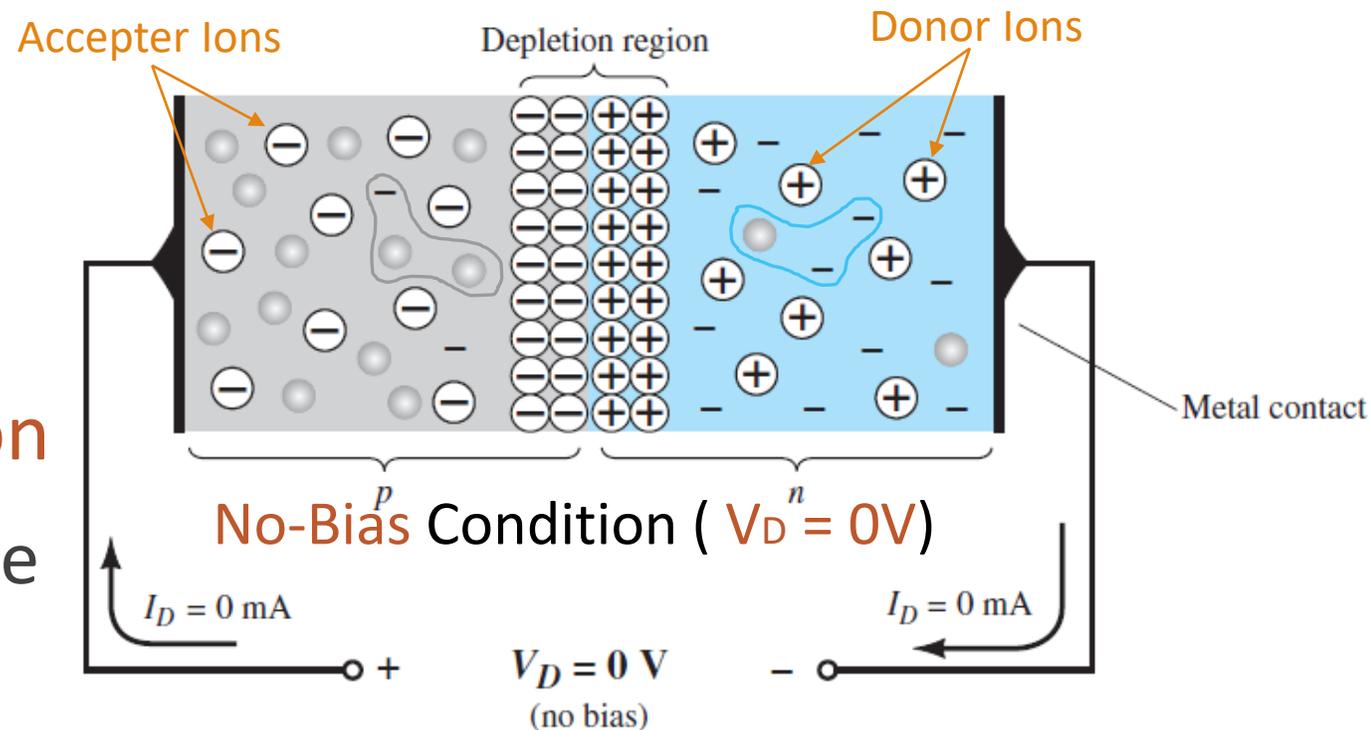
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1. pn-junction and the semiconductor Diode
2. Diode Characteristic Graph (IV-Curve)
3. Temperature Effects
4. Diode Resistance Types
5. Examples
6. Reading Assignment

# pn-junction and the semiconductor Diode

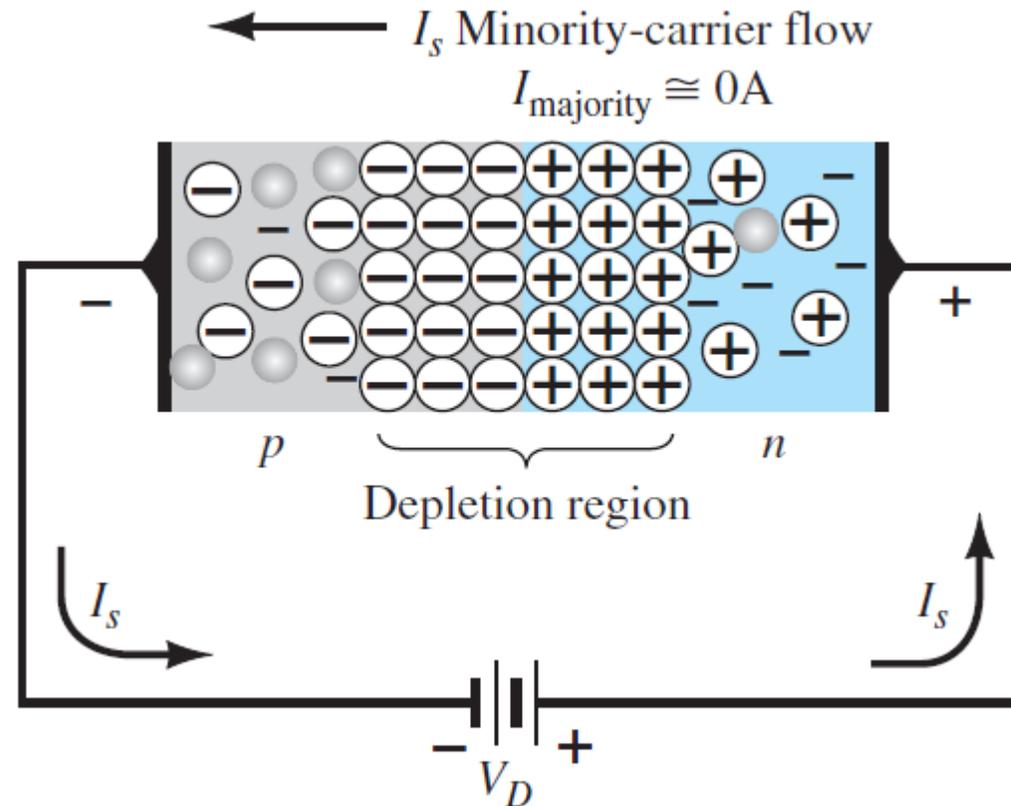
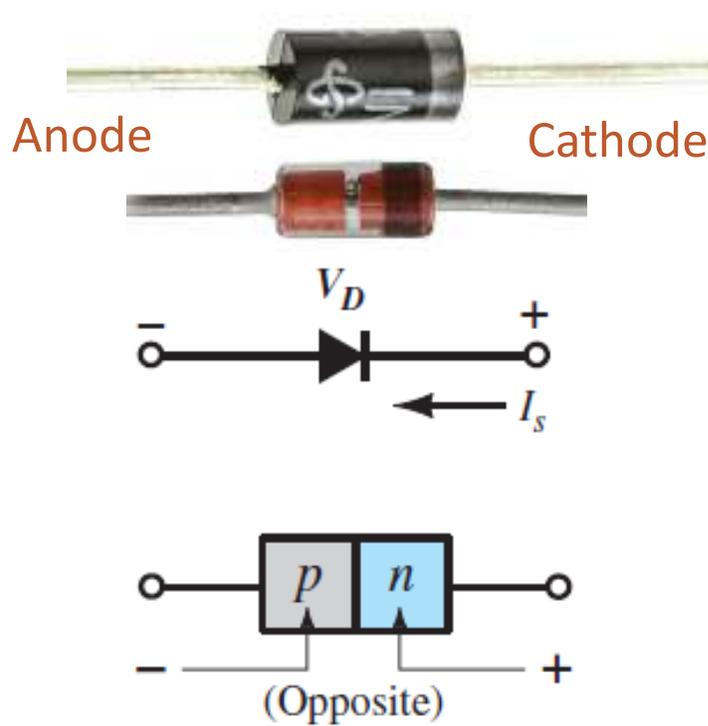
- Joining p-type material with a majority carrier of holes to n-type with a majority carrier of electrons forms the semiconductor diode.

- Depletion region:  
lack of free carriers in the region near the junction
- the net flow of charge in one direction is zero for  $V_D = 0V$ .



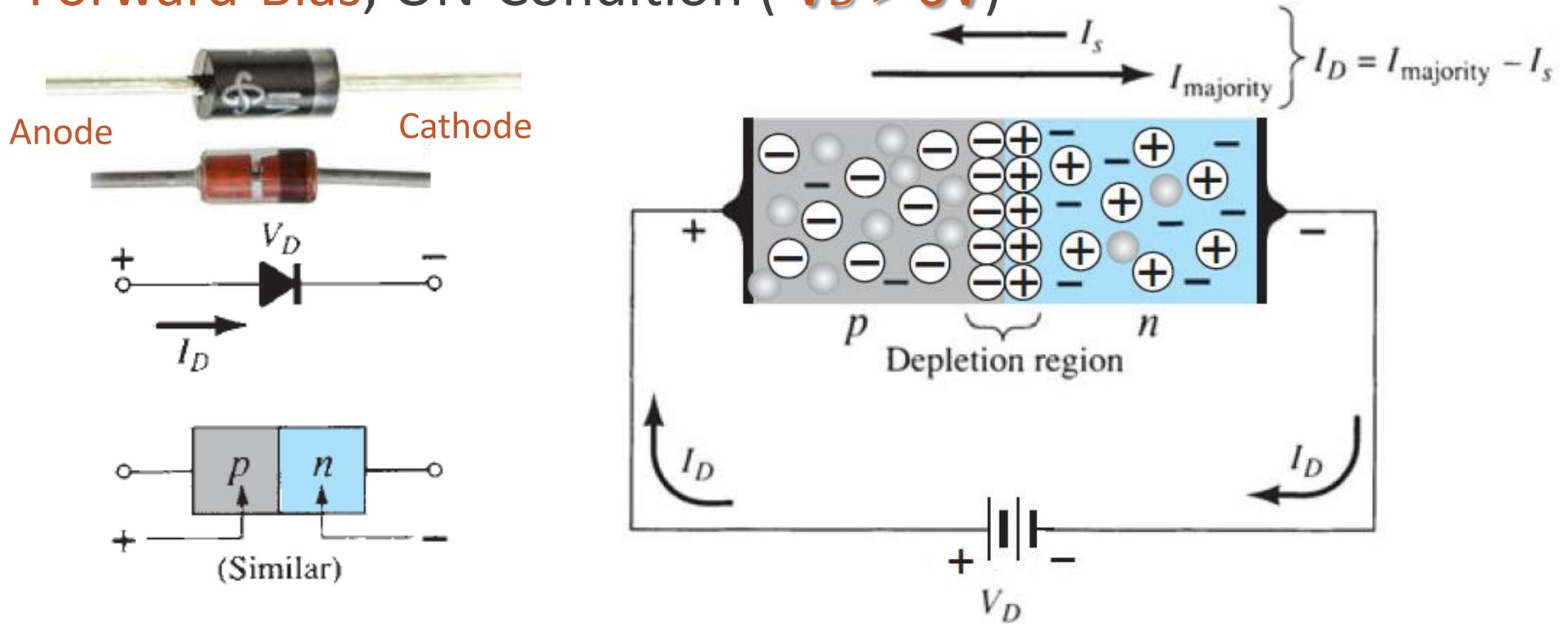
# pn-junction and the semiconductor Diode (cont'd)

Reverse-Bias; OFF-Condition ( $V_D < 0V$ )



# pn-junction and the semiconductor Diode (cont'd)

Forward-Bias; ON-Condition ( $V_D > 0V$ )



# Diode Characteristic Graph (IV-Curve)

- The general characteristics of a semiconductor diode can be defined by **Shockley's** equation for the **forward**- and **reverse-bias** regions:

$$I_D = I_S(e^{V_D/nV_T} - 1) \quad (A)$$

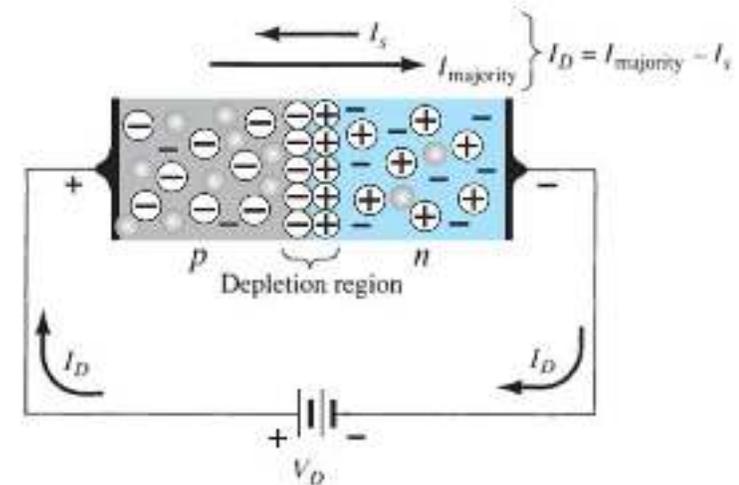
Where:

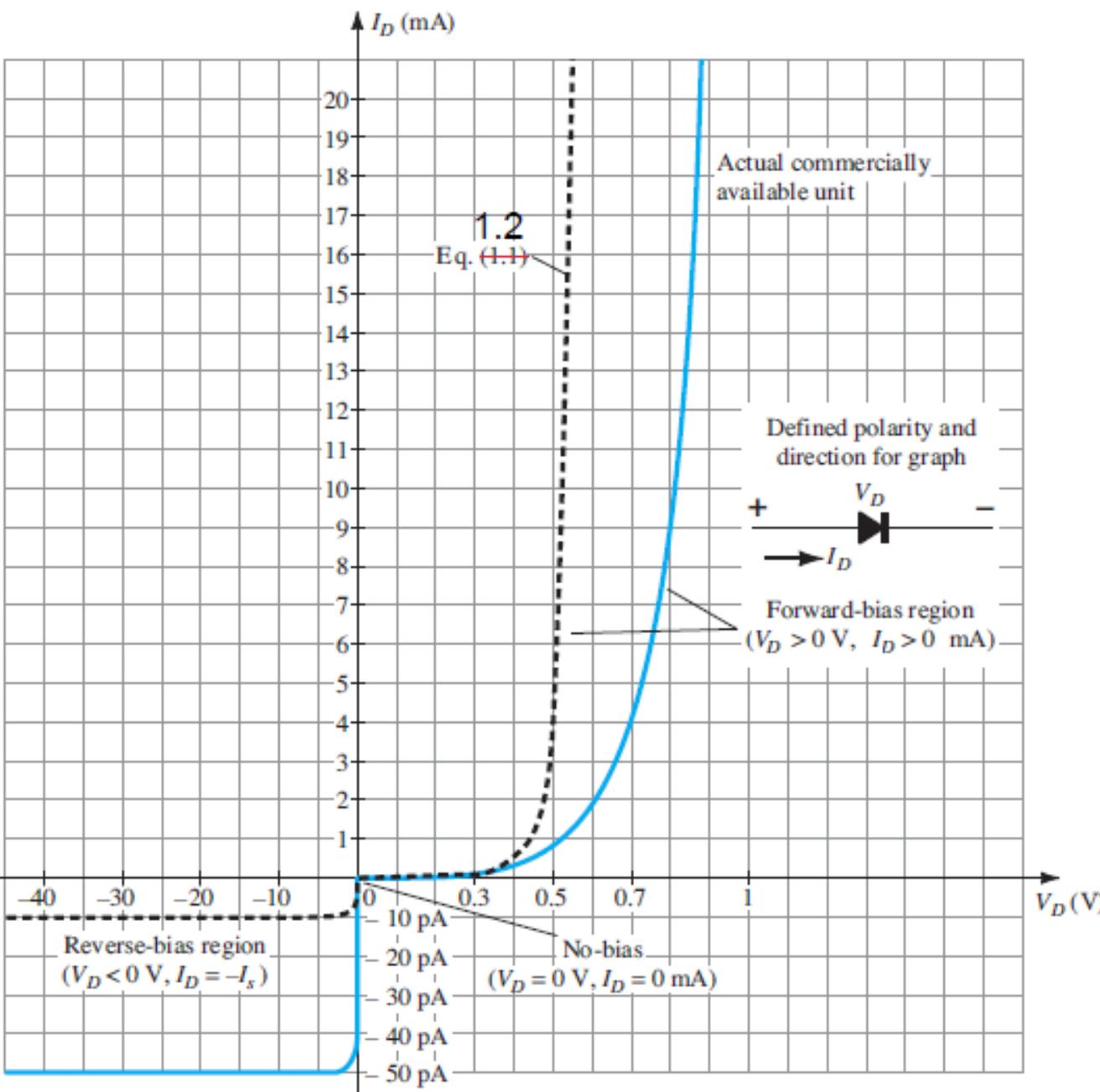
$I_S$  is the **reverse saturation current**.

$V_D$  is the forward-bias voltage across the diode.

$n$  is an **ideality factor**; it has a range between 1 and 2. (a measure of how closely the diode follows the ideal diode equation)

$V_T$  is called the **thermal voltage**.





Remarks:  $I_D = I_s e^{V_D/nV_T} - I_s$

- As the value of  $V_D$  increases, the curve becomes almost vertical.

$$I_D \cong I_s e^{V_D/nV_T} \quad (V_D \text{ positive})$$

- For negative values of  $V_D$ , the exponential term drops very quickly below the level of  $I_D$ .

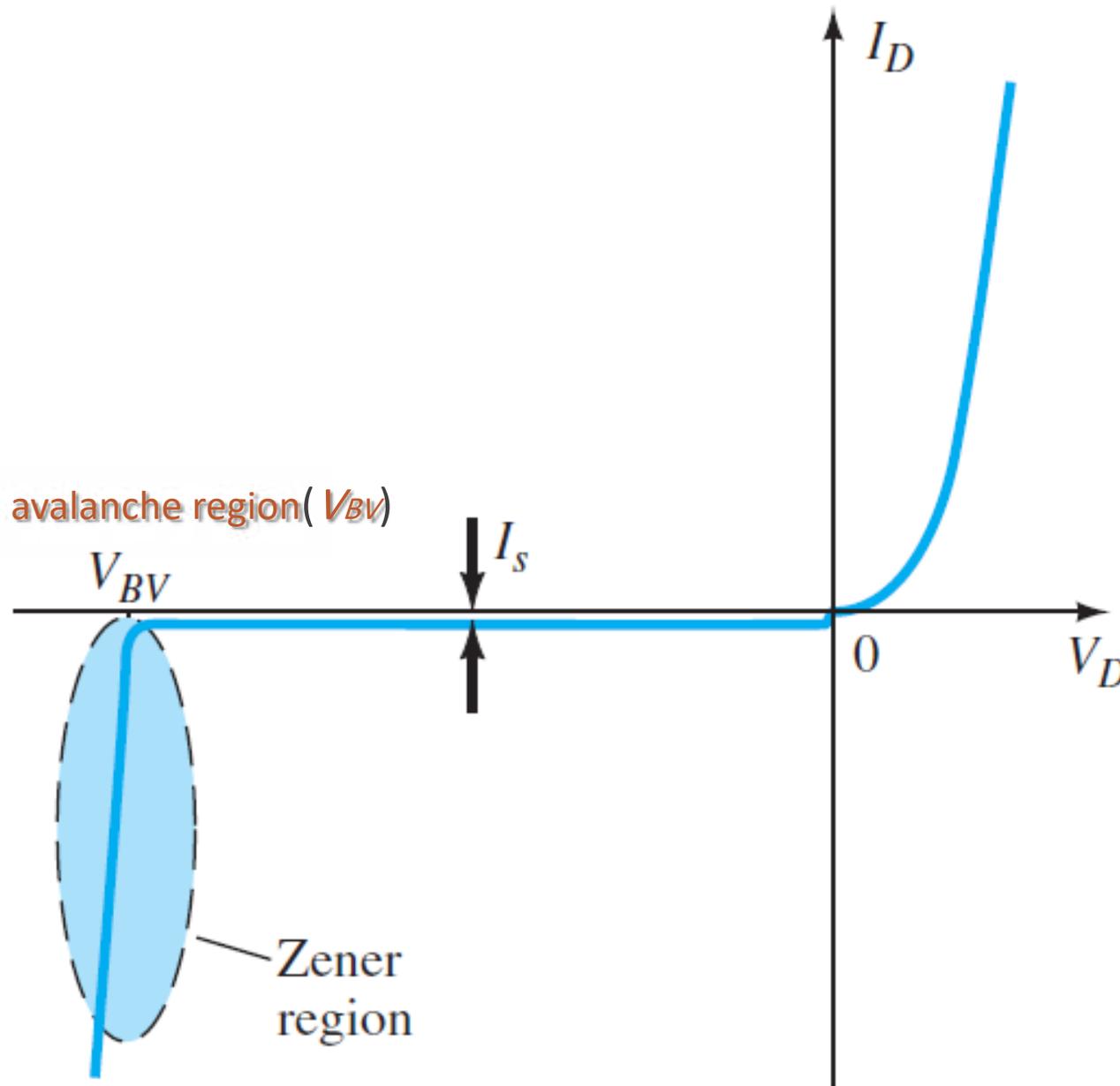
$$I_D \cong -I_s \quad (V_D \text{ negative})$$

- At  $V_D = 0$  V,  $I_D = I_s(e^0 - 1) = I_s(1 - 1) = 0$

- Commercially available silicon diodes deviate from the ideal Diode (internal “body” resistance, external “contact” resistance of a diode.)

- The actual  $I_s$  of a commercially available diode will normally be measurably larger than that in Shockley’s equation.

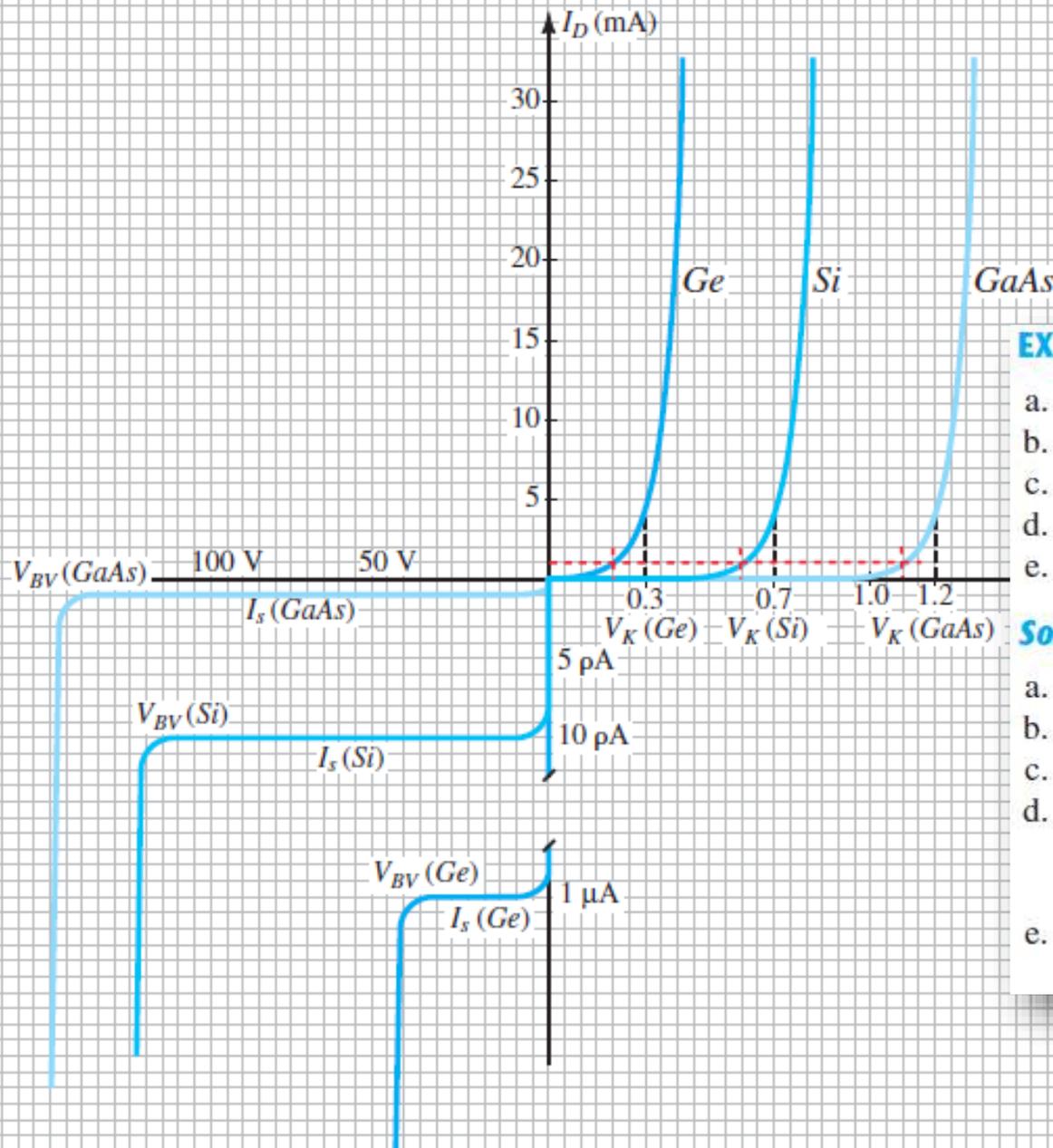
# Diode Characteristic Graph (IV-Curve) (cont'd)



- Applying negative voltage with the **reverse polarity** will result in a sharp change in the characteristics called breakdown potential ( $V_{BV}$ )
- The **avalanche region** can be brought closer to the vertical axis by **increasing the doping** levels in the p- and n-type materials.
- Decreasing  $V_{BV}$  to a very low level, such as -5V, another mechanism called **Zener breakdown** will contribute to the sharp change in the characteristic.
- The maximum **reverse bias** that can be applied before entering the **breakdown region** is called the **peak inverse voltage (PIV rating)** or the **peak reverse voltage (PRV rating)**.

**TABLE 1.3**
*Knee Voltages  $V_K$* 

Semiconductor	$V_K$ (V)
Ge	0.3
Si	0.7
GaAs	1.2


**EXAMPLE 1.2**

- Determine the voltage across each diode at a current of 1 mA.
- Repeat for a current of 4 mA.
- Repeat for a current of 30 mA.
- Determine the average value of the diode voltage for the range of currents listed above.
- How do the average values compare to the knee voltages listed in Table 1.3?

**Solution:**

- $V_D(\text{Ge}) = 0.2 \text{ V}$ ,  $V_D(\text{Si}) = 0.6 \text{ V}$ ,  $V_D(\text{GaAs}) = 1.1 \text{ V}$
- $V_D(\text{Ge}) = 0.3 \text{ V}$ ,  $V_D(\text{Si}) = 0.7 \text{ V}$ ,  $V_D(\text{GaAs}) = 1.2 \text{ V}$
- $V_D(\text{Ge}) = 0.42 \text{ V}$ ,  $V_D(\text{Si}) = 0.82 \text{ V}$ ,  $V_D(\text{GaAs}) = 1.33 \text{ V}$
- Ge:  $V_{\text{av}} = (0.2 \text{ V} + 0.3 \text{ V} + 0.42 \text{ V})/3 = 0.307 \text{ V}$

Si:  $V_{\text{av}} = (0.6 \text{ V} + 0.7 \text{ V} + 0.82 \text{ V})/3 = 0.707 \text{ V}$

GaAs:  $V_{\text{av}} = (1.1 \text{ V} + 1.2 \text{ V} + 1.33 \text{ V})/3 = 1.21 \text{ V}$
- Very close correspondence. Ge: 0.307 V vs. 0.3 V, Si: 0.707 V vs. 0.7 V, GaAs: 1.21 V vs. 1.2 V.

# Diode Resistance types

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Diode resistance is **variable** due to the **nonlinear** shape of the characteristic curve.

## 1. DC (Static) Resistance

$$R_D = \frac{V_D}{I_D}$$

## 2. AC (Dynamic) Resistance

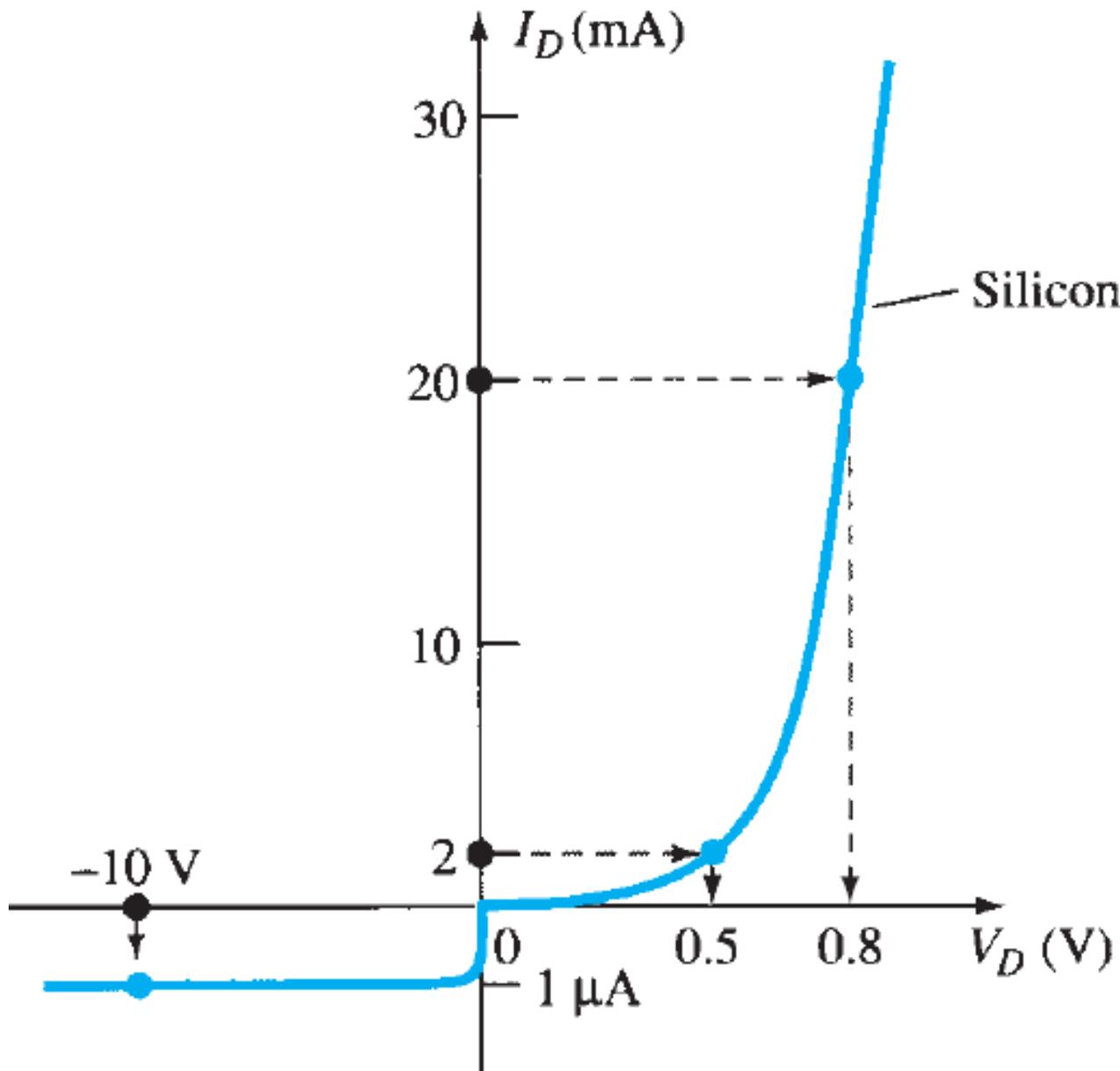
$$r_d = \frac{\Delta V_d}{\Delta I_d}$$

$$r_d = \frac{26 \text{ mV}}{I_D}$$

## 3. Average AC Resistance

$$r_{av} = \left. \frac{\Delta V_d}{\Delta I_d} \right|_{\text{pt. to pt.}}$$

# Examples



**EXAMPLE 1.3** Determine the dc resistance levels for the diode

- $I_D = 2$  mA (low level)
- $I_D = 20$  mA (high level)
- $V_D = -10$  V (reverse-biased)

**Solution:**

- At  $I_D = 2$  mA,  $V_D = 0.5$  V (from the curve) and

$$R_D = \frac{V_D}{I_D} = \frac{0.5 \text{ V}}{2 \text{ mA}} = 250 \Omega$$

- At  $I_D = 20$  mA,  $V_D = 0.8$  V (from the curve) and

$$R_D = \frac{V_D}{I_D} = \frac{0.8 \text{ V}}{20 \text{ mA}} = 40 \Omega$$

- At  $V_D = -10$  V,  $I_D = -I_s = -1 \mu\text{A}$  (from the curve) and

$$R_D = \frac{V_D}{I_D} = \frac{10 \text{ V}}{1 \mu\text{A}} = 10 \text{ M}\Omega$$

*The higher the current through a diode, the lower the dc resistance level*

# Outline

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1. Diode Equivalent Circuits
2. Diode Load Line Analysis (aka **graphical solution**)
3. Series Diode Configurations
4. Parallel and Series-Parallel Configurations
5. Tutorial
6. Reading Assignment

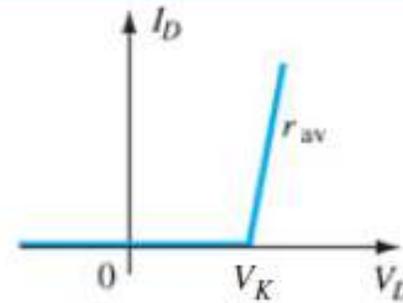
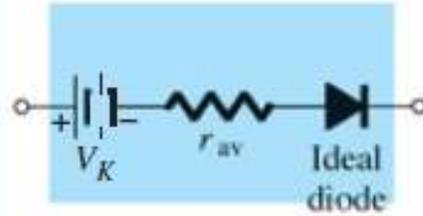
Type

Conditions

Model

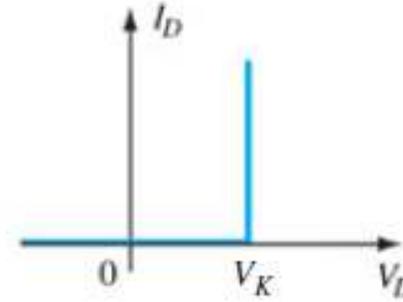
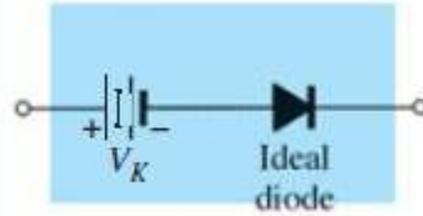
Characteristics

Piecewise-linear model



Simplified model

$$R_{\text{network}} \gg r_{\text{av}}$$



Ideal device

$$R_{\text{network}} \gg r_{\text{av}}$$

$$E_{\text{network}} \gg V_K$$

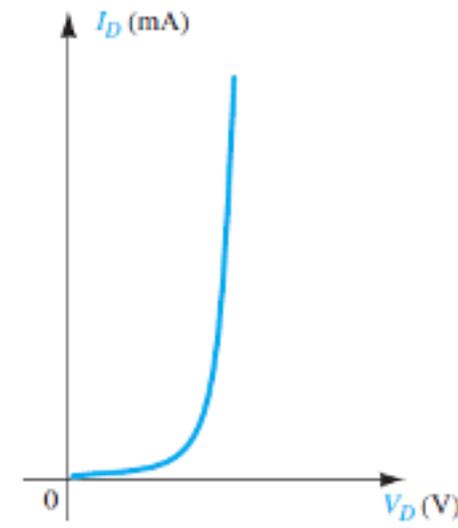
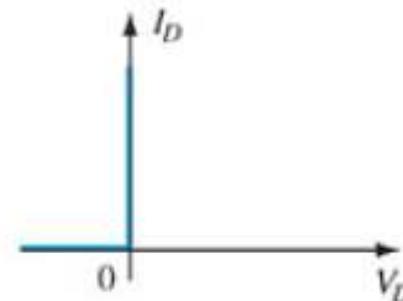
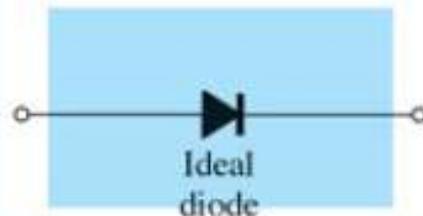


TABLE 1.3

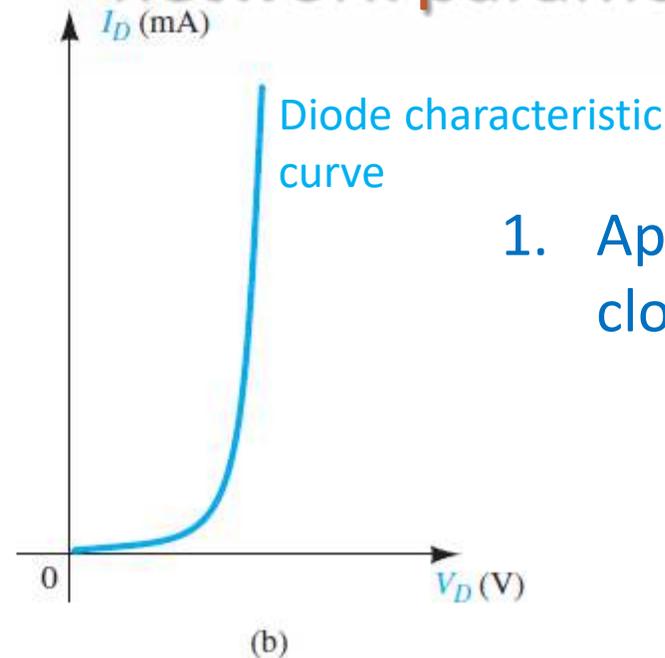
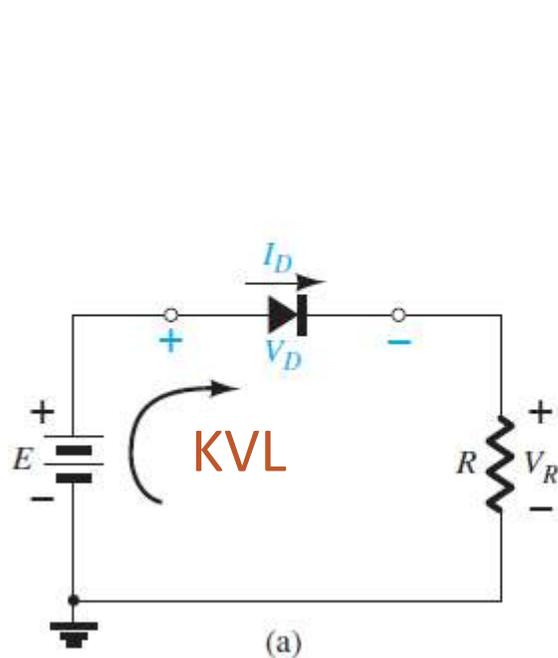
Knee Voltages  $V_K$

Semiconductor	$V_K$ (V)
Ge	0.3
Si	0.7
GaAs	1.2

$$r_{\text{av}} = \left. \frac{\Delta V_d}{\Delta I_d} \right|_{\text{pt. to pt.}}$$

# Diode Load Line Analysis (graphical solution)

- Load line analysis is used to find the **current** and **voltage** levels of the diode that will **satisfy both** the **characteristics** of the diode and the **network parameters** simultaneously.

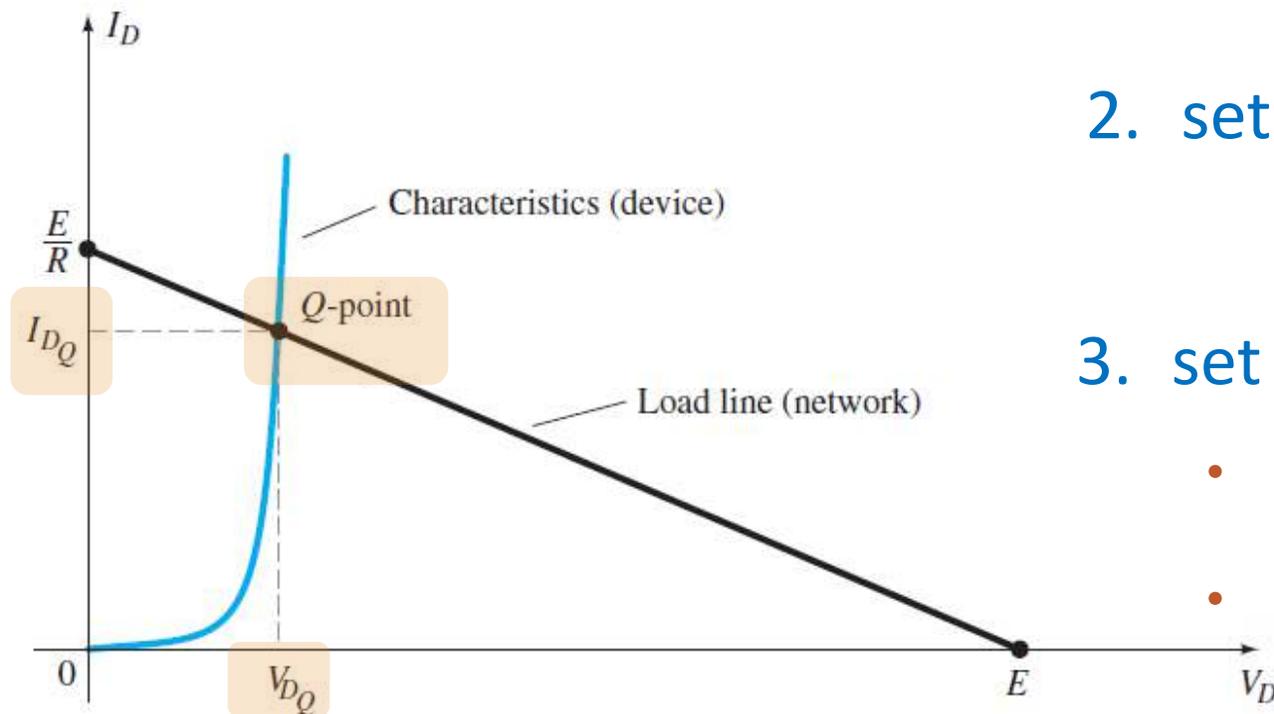


1. Apply Kirchhoff's voltage law in the clockwise direction:

$$E = V_D + I_D R$$

# Diode Load Line Analysis (cont'd)

- The diode **characteristics** are placed **on the same set of axes** as a **straight line** defined by the parameters of the network.



2. set  $V_D = 0V$ , 
$$I_D = \frac{E}{R} \Big|_{V_D=0V}$$

3. set  $I_D = 0A$ , 
$$V_D = E \Big|_{I_D=0A}$$

- We now have a load line defined by the **network** and a characteristic curve defined by the **device**.
- The point of **operation** (intersection) is called the **quiescent point (Q-point)**

# Diode Load Line Analysis (cont'd)

---

- The solution obtained at the **intersection** of the two curves is **the same** as would be obtained by a **simultaneous mathematical solution** of:

$$I_D = \frac{E}{R} - \frac{V_D}{R}$$

and

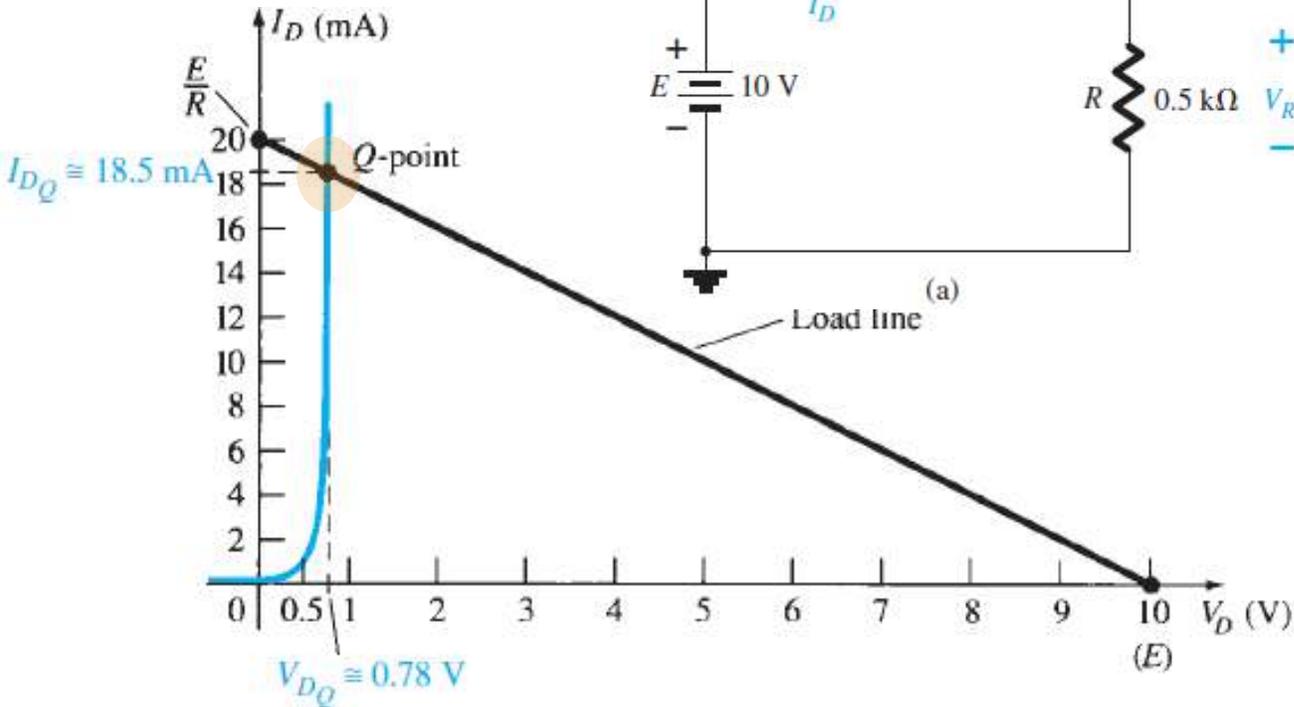
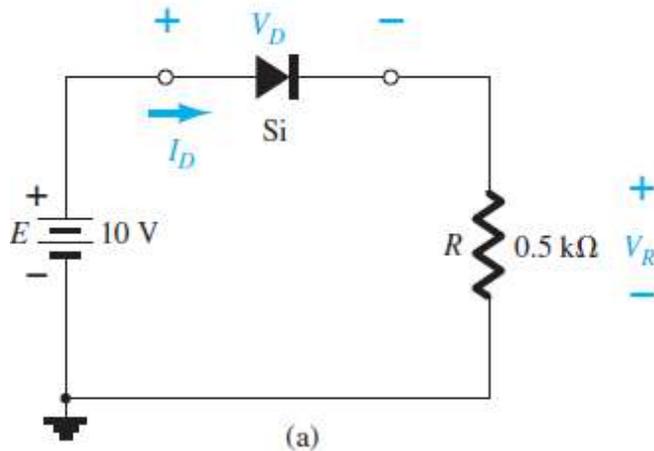
$$I_D = I_S(e^{V_D/nV_T} - 1)$$

- The curve for a diode has **nonlinear characteristics**. Therefore, the mathematics involved would require using **nonlinear techniques**.

# Diode Load Line Analysis (cont'd)

**EXAMPLE 2.1** For the series diode configuration of Fig. 2.3a, employing the diode characteristics of Fig. 2.3b, determine:

- a.  $V_{DQ}$  and  $I_{DQ}$ .
- b.  $V_R$ .



**Solution:**

a. 
$$I_D = \left. \frac{E}{R} \right|_{V_D=0\text{ V}} = \frac{10\text{ V}}{0.5\text{ k}\Omega} = 20\text{ mA}$$

$$V_D = E \Big|_{I_D=0\text{ A}} = 10\text{ V}$$

the Q-point is:

$$V_{DQ} \cong 0.78\text{ V}$$

$$I_{DQ} \cong 18.5\text{ mA}$$

b. 
$$V_R = E - V_D = 10\text{ V} - 0.78\text{ V} = 9.22\text{ V}$$

# Diode Load Line Analysis (cont'd)

**EXAMPLE 2.2** Repeat Example 2.1 using the **approximate** equivalent model for the silicon semiconductor diode.

**Solution:**

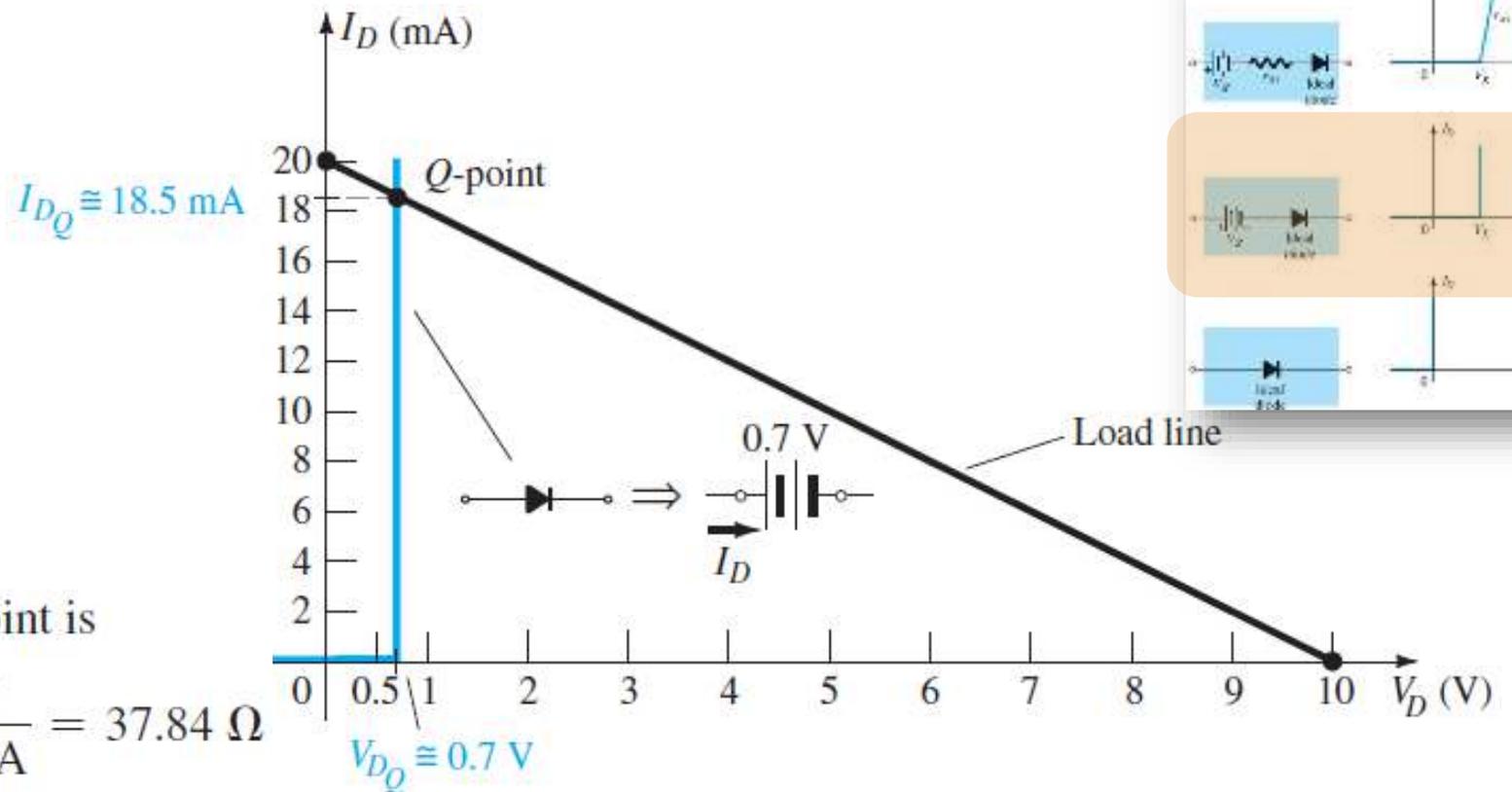
$$V_{DQ} = 0.7 \text{ V}$$

$$I_{DQ} = 18.5 \text{ mA}$$

**Note:**

For this situation the dc resistance of the Q-point is

$$R_D = \frac{V_{DQ}}{I_{DQ}} = \frac{0.7 \text{ V}}{18.5 \text{ mA}} = 37.84 \ \Omega$$



# Diode Load Line Analysis (cont'd)

**EXAMPLE 2.3** Repeat Example 2.1 using the **ideal diode model**.

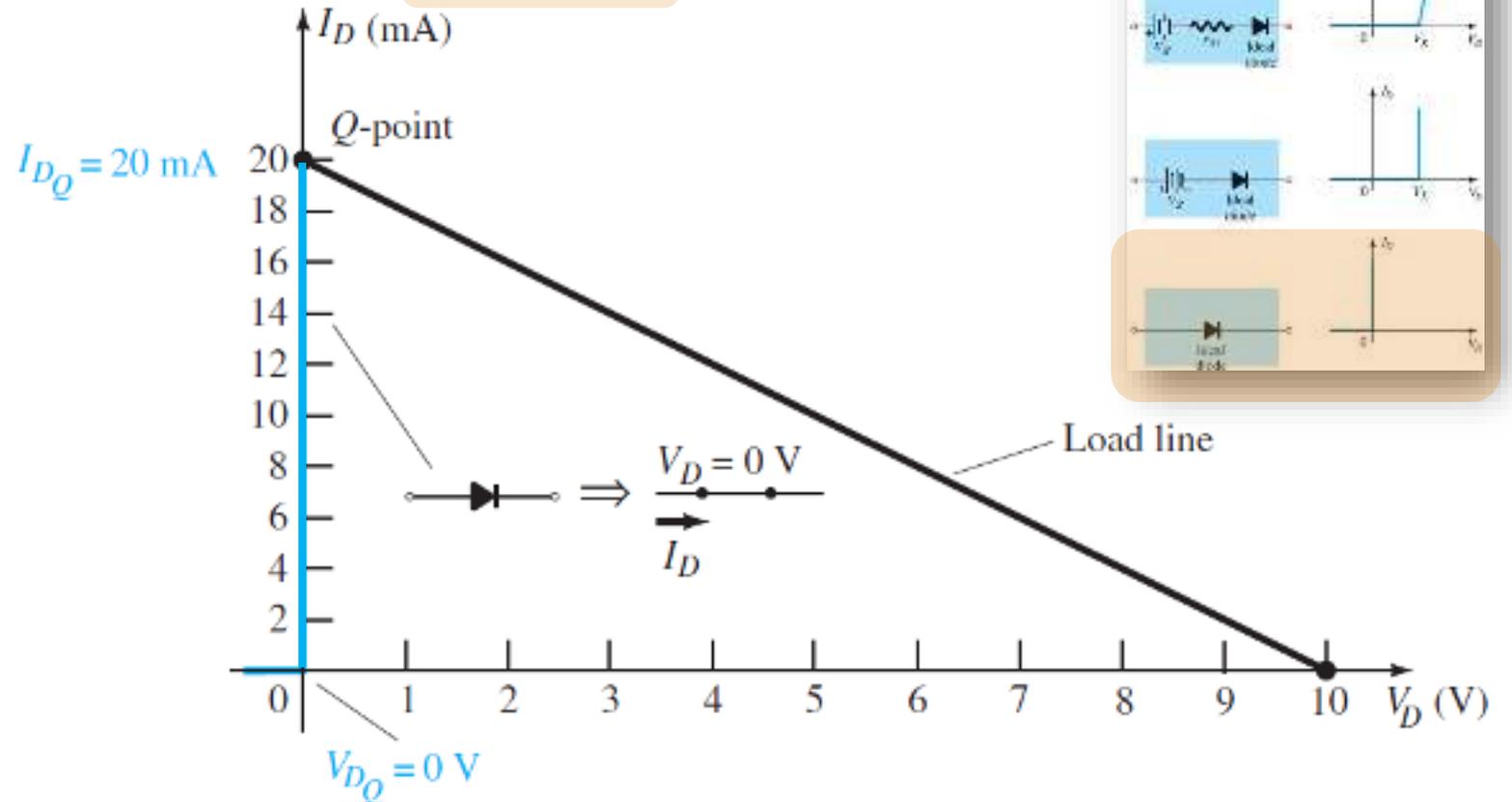
**Solution:**

$$V_{DQ} = 0 \text{ V}$$

$$I_{DQ} = 20 \text{ mA}$$

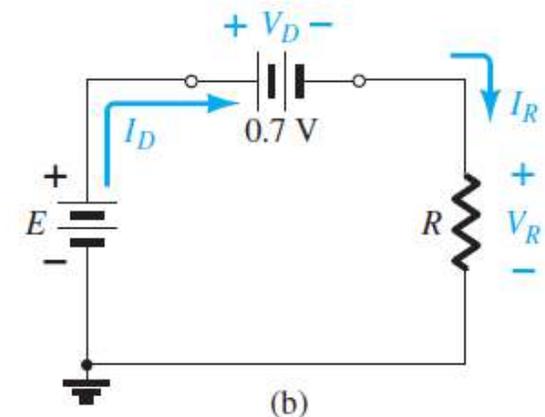
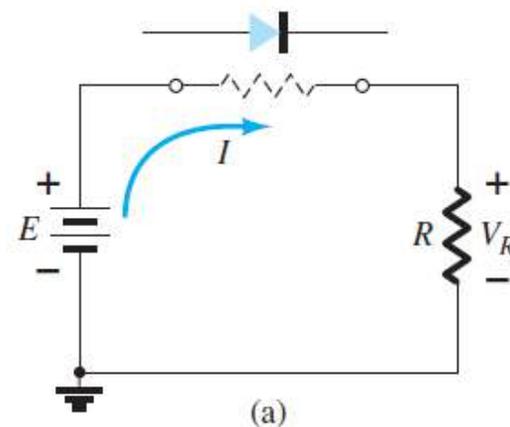
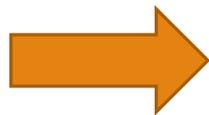
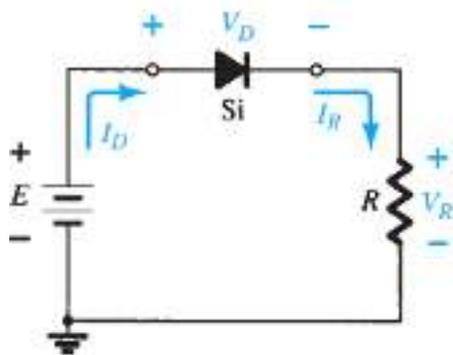
**Note:**

$$R_D = \frac{V_{DQ}}{I_{DQ}} = \frac{0 \text{ V}}{20 \text{ mA}} = 0 \Omega$$



# Series Diode Configurations

- The state of the diode is first determined by **mentally replacing** the diode with a **resistive** element.
- If the resulting direction of ( $I$ ) matches the **arrow** in the diode symbol, and  $E > V_K$ , the diode is in the “**on**” state.
- The network is then **redrawn** with the appropriate **equivalent model** for the forward-biased silicon diode.

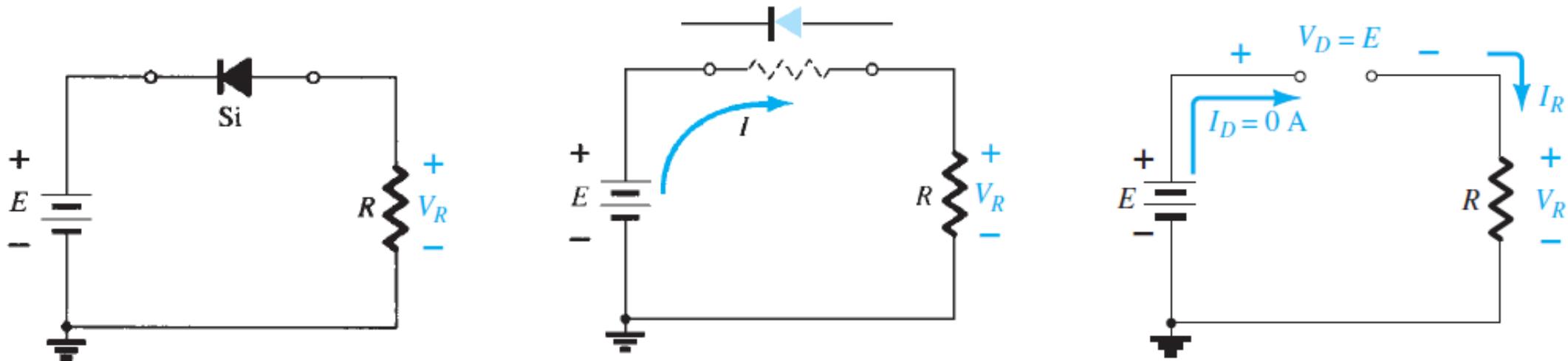


# Series Diode Configurations (cont'd)

$$V_R = E - V_K$$

$$I_D = I_R = \frac{V_R}{R}$$

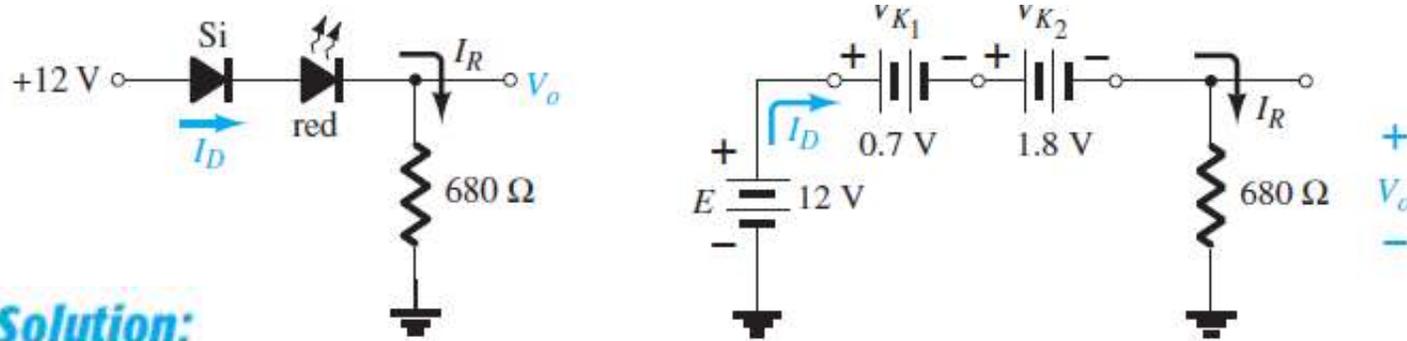
- If the resulting direction of  $I$  is **opposite** to the **arrow** in the diode symbol, the diode is in the “**off**” state, and  $V_R = I_R R = I_D R = (0A)R = 0V$





# Series Diode Configurations (cont'd)

**EXAMPLE 2.7** Determine  $V_o$  and  $I_D$  for the series circuit



**Solution:**

$$E = 12\text{V} > 2.5\text{V} \quad (0.7\text{V} + 1.8\text{V})$$

$$V_o = E - V_{K_1} - V_{K_2} = 12\text{V} - 2.5\text{V} = 9.5\text{V}$$

$$I_D = I_R = \frac{V_R}{R} = \frac{V_o}{R} = \frac{9.5\text{V}}{680\ \Omega} = 13.97\text{ mA}$$

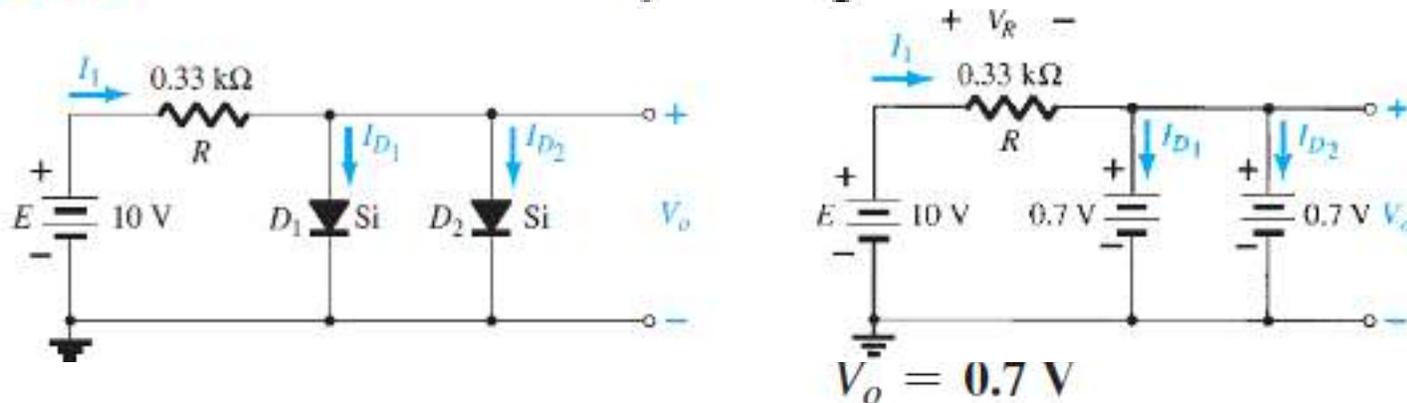
**TABLE 1.9**  
Light-Emitting Diodes

Color	Construction	Typical Forward Voltage (V)
Amber	AllnGaP	2.1
Blue	GaN	5.0
Green	GaP	2.2
Orange	GaAsP	2.0
Red	GaAsP	1.8
White	GaN	4.1
Yellow	AllnGaP	2.1

**AllnGaP:** Aluminum gallium indium phosphide  
**GaAsP:** Gallium Arsenide Phosphide

# Parallel and Series-Parallel Configurations

**EXAMPLE 2.10** Determine  $V_o$ ,  $I_1$ ,  $I_{D_1}$ , and  $I_{D_2}$  for the parallel diode configuration



**Solution:**

The current is

$$I_1 = \frac{V_R}{R} = \frac{E - V_D}{R} = \frac{10 \text{ V} - 0.7 \text{ V}}{0.33 \text{ k}\Omega} = 28.18 \text{ mA}$$

Assuming diodes of similar characteristics, we have

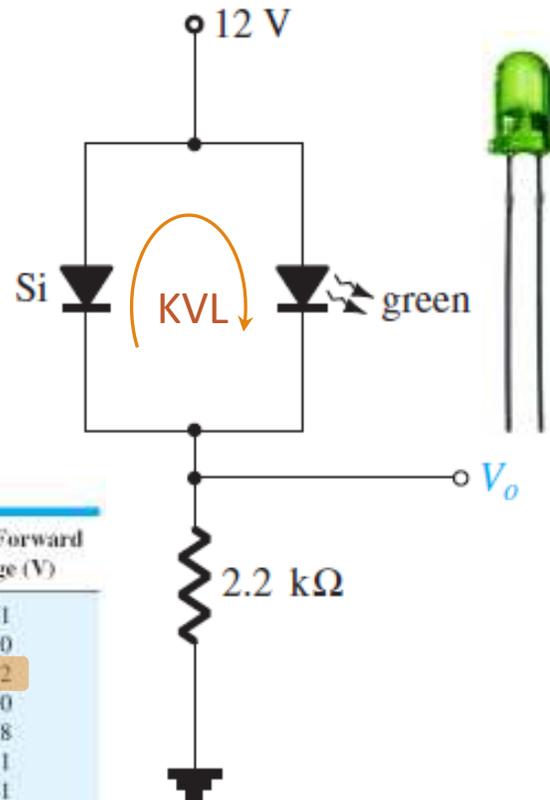
$$I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18 \text{ mA}}{2} = 14.09 \text{ mA}$$

Since the resulting current direction matches that of the arrow in each diode symbol and the applied voltage is greater than 0.7 V, both diodes are in the “on” state.

The reason for placing diodes in parallel is to increase the current rating of the diodes.

# Parallel and Series-Parallel Configurations (cont'd)

**EXAMPLE 2.12** Determine the voltage  $V_o$  for the network



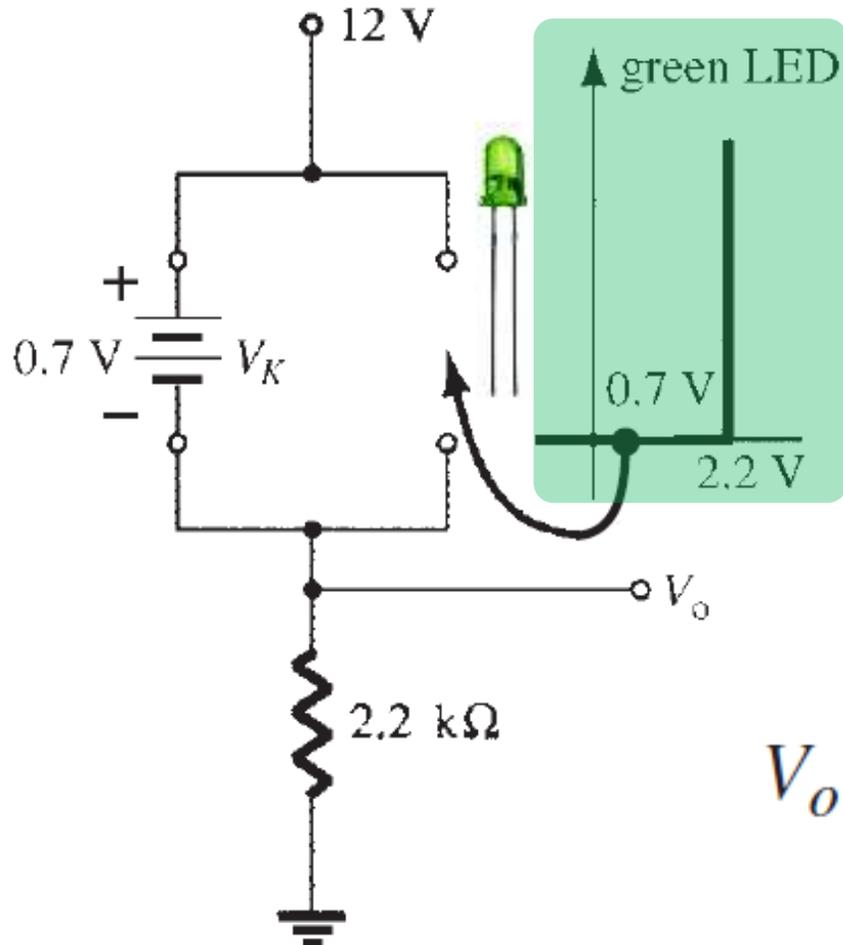
**TABLE 1.9**  
Light-Emitting Diodes

Color	Construction	Typical Forward Voltage (V)
Amber	AlInGaP	2.1
Blue	GaN	5.0
Green	GaP	2.2
Orange	GaAsP	2.0
Red	GaAsP	1.8
White	GaN	4.1
Yellow	AlInGaP	2.1

- **Note:** If both diodes were ON, there would be **more than one voltage** across the parallel diodes, **violating** one of the basic rules of network analysis:

*The voltage must be the same across parallel elements.*

# Parallel and Series-Parallel Configurations (cont'd)



- The result is that the voltage across the green LED **will never rise above 0.7 V** and will remain in the equivalent **open-circuit state**.

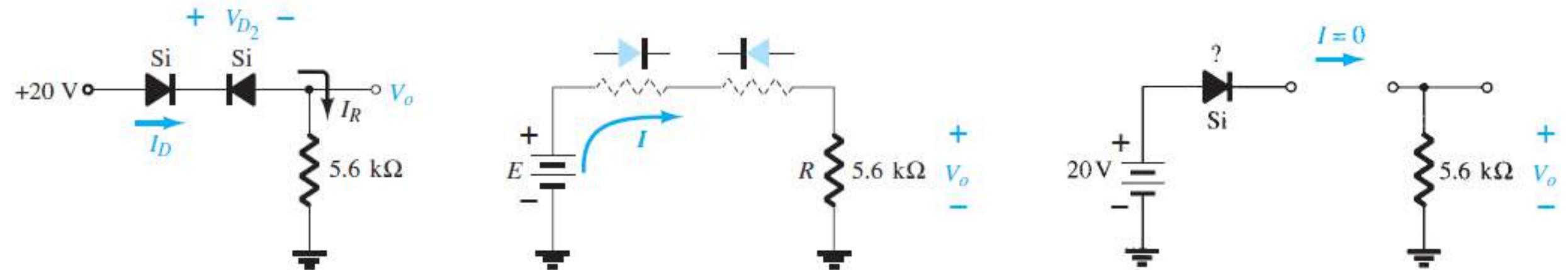
$$V_o = 12 \text{ V} - 0.7 \text{ V} = \mathbf{11.3 \text{ V}}$$

# Tutorial

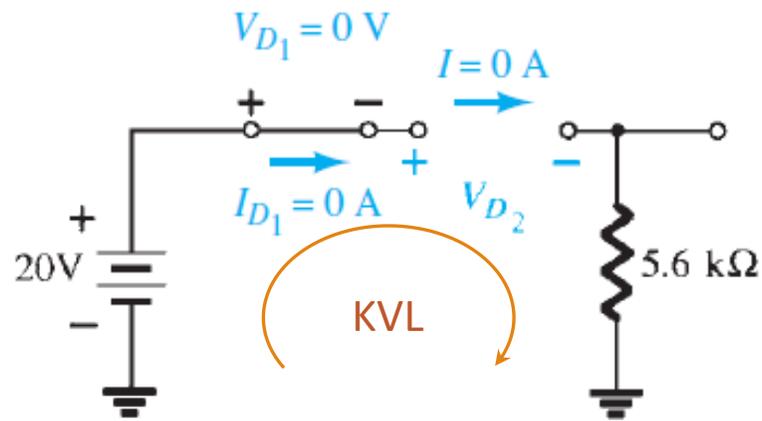
**EXAMPLE 2.8** Determine  $I_D$ ,  $V_{D_2}$ , and  $V_o$  for the circuit

**Solution:**

The combination of a short circuit in series with an open circuit always results in an **open circuit** and  $I_D = 0A$ .



# Tutorial (Example 2.8 cont'd)



recall for the actual practical diode that when  $I_D = 0A$ ,  $V_D = 0V$  (and vice versa)

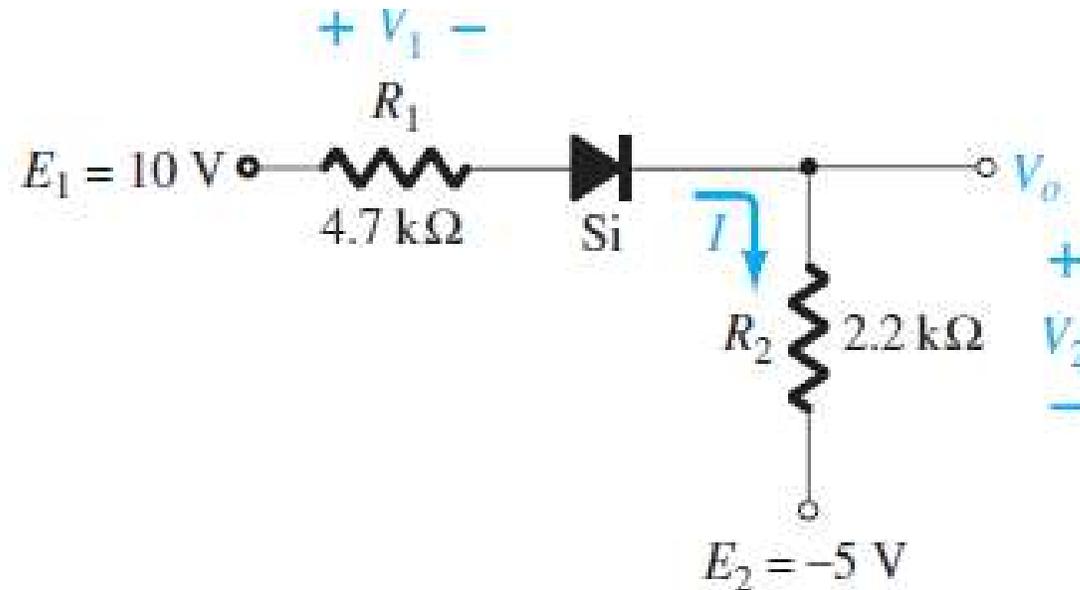
$$\begin{aligned} V_o &= I_R R = I_D R = (0A)R = \mathbf{0V} \\ V_{D_2} &= V_{\text{open circuit}} = E = \mathbf{20V} \end{aligned}$$

Applying Kirchhoff's voltage law in a clockwise direction gives

$$\begin{aligned} E - V_{D_1} - V_{D_2} - V_o &= 0 \\ V_{D_2} &= E - V_{D_1} - V_o = 20V - 0 - 0 \\ &= \mathbf{20V} \\ V_o &= \mathbf{0V} \end{aligned}$$

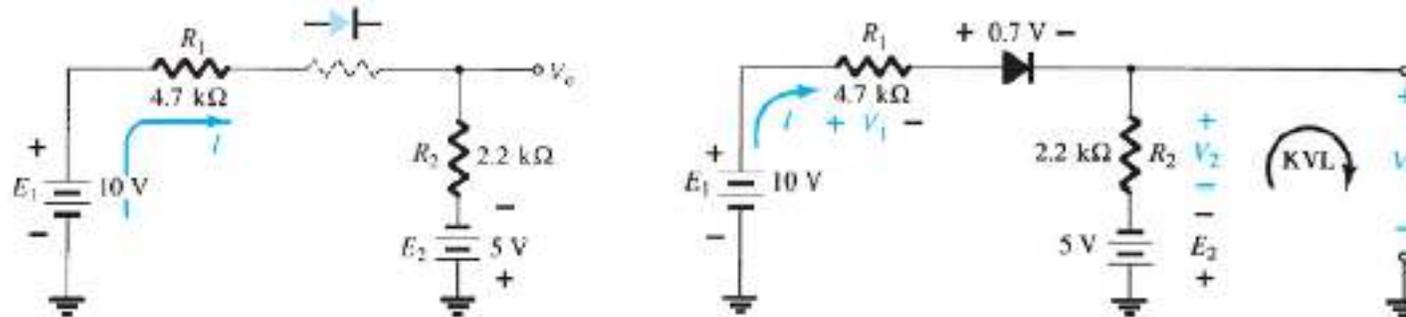
# Tutorial

**EXAMPLE 2.9** Determine  $I$ ,  $V_1$ ,  $V_2$ , and  $V_o$  for the series dc configuration



# Tutorial (Example 2.9 cont'd)

**Solution:**



The resulting current through the circuit is

$$I = \frac{E_1 + E_2 - V_D}{R_1 + R_2} = \frac{10 \text{ V} + 5 \text{ V} - 0.7 \text{ V}}{4.7 \text{ k}\Omega + 2.2 \text{ k}\Omega} = \frac{14.3 \text{ V}}{6.9 \text{ k}\Omega}$$

$$\cong \mathbf{2.07 \text{ mA}}$$

and the voltages are

$$V_1 = IR_1 = (2.07 \text{ mA})(4.7 \text{ k}\Omega) = \mathbf{9.73 \text{ V}}$$

$$V_2 = IR_2 = (2.07 \text{ mA})(2.2 \text{ k}\Omega) = \mathbf{4.55 \text{ V}}$$

Applying Kirchhoff's voltage law to the output section in the clockwise direction results in

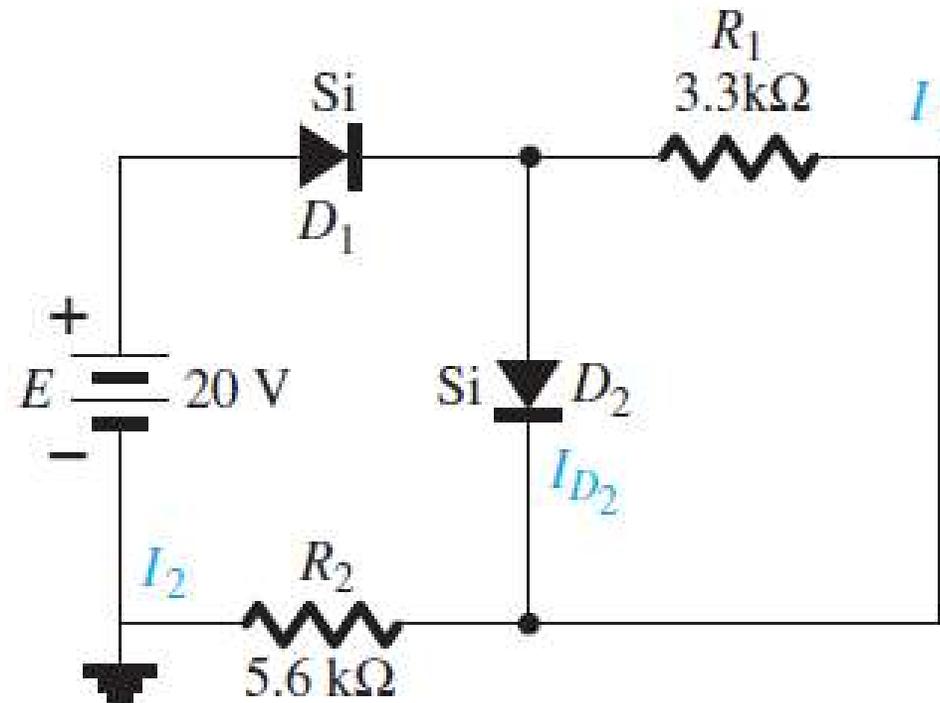
$$-E_2 + V_2 - V_o = 0$$

and

$$V_o = V_2 - E_2 = 4.55 \text{ V} - 5 \text{ V} = \mathbf{-0.45 \text{ V}}$$

# Tutorial

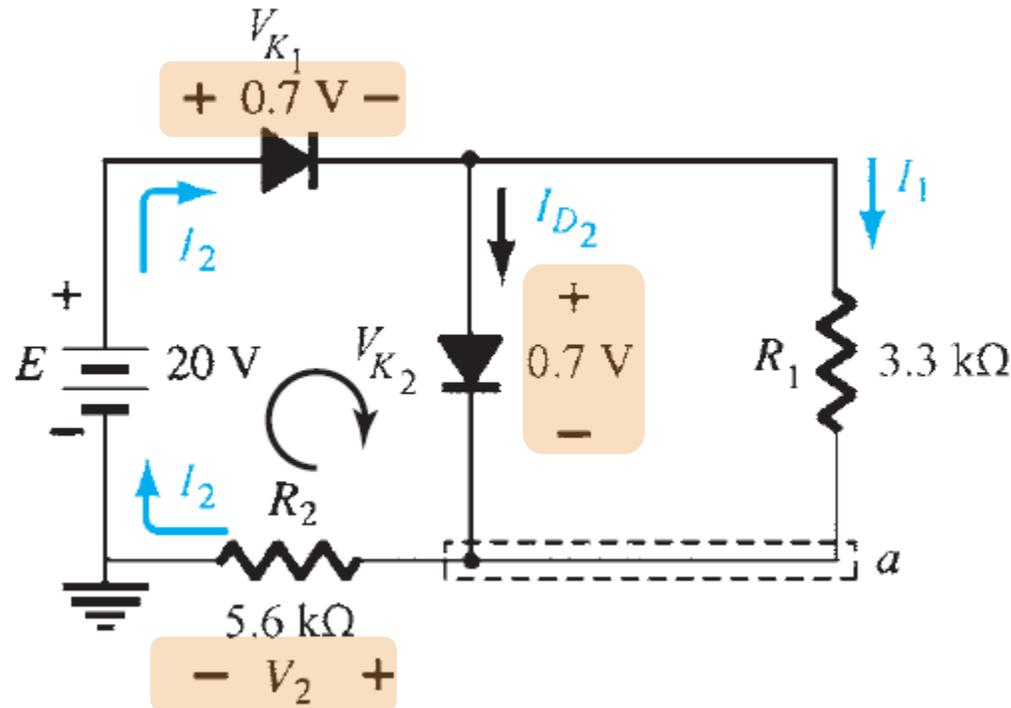
**EXAMPLE 2.13** Determine the currents  $I_1$ ,  $I_2$ , and  $I_{D_2}$  for the network



# Tutorial (Example 2.13 cont'd)

## Solution:

The applied voltage is such as to turn **both diodes on**, as indicated by the resulting current directions in the network.



$$I_1 = \frac{V_{K_2}}{R_1} = \frac{0.7\text{ V}}{3.3\text{ k}\Omega} = \mathbf{0.212\text{ mA}}$$

# Tutorial (Example 2.13 cont'd)

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Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction yields

$$-V_2 + E - V_{K_1} - V_{K_2} = 0$$

and  $V_2 = E - V_{K_1} - V_{K_2} = 20 \text{ V} - 0.7 \text{ V} - 0.7 \text{ V} = \mathbf{18.6 \text{ V}}$

with  $I_2 = \frac{V_2}{R_2} = \frac{18.6 \text{ V}}{5.6 \text{ k}\Omega} = \mathbf{3.32 \text{ mA}}$

At the bottom node  $a$ ,

$$I_{D_2} + I_1 = I_2$$

and  $I_{D_2} = I_2 - I_1 = 3.32 \text{ mA} - 0.212 \text{ mA} \cong \mathbf{3.11 \text{ mA}}$